

# ADM3-00001PD

## 300 kHz – 18 GHz Broadband High-Gain Amplifier

### DEVICE OVERVIEW

#### General Description

The ADM3-00001PD is a high-gain, broadband 3-stage amplifier capable of providing +21 dBm output power up to 18 GHz. This amplifier features a flat group delay, fast rise time response, and low noise figure. This product is an unprotected amplifier module intended for lab use.



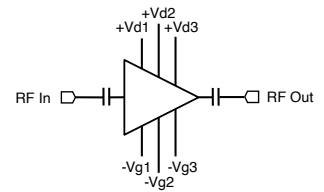
#### Features

- +23 dBm output power
- +37 dB gain
- Flat group delay response

#### Applications

- Test and Measurement Equipment
- LO Driver Amplifier

#### Functional Block Diagram



#### Part Ordering Options

Part Number	Description	Package	Connectors	Green Status	Product Lifecycle	Export Classification
ADM3-00001PD	300 kHz – 18 GHz Broadband High-Gain Amplifier	PD	<u>Standard</u>	REACH RoHS	Released	EAR99

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### Revision History

Revision Code	Revision Date	Comment
-	2022-12-01	Datasheet Initial Release

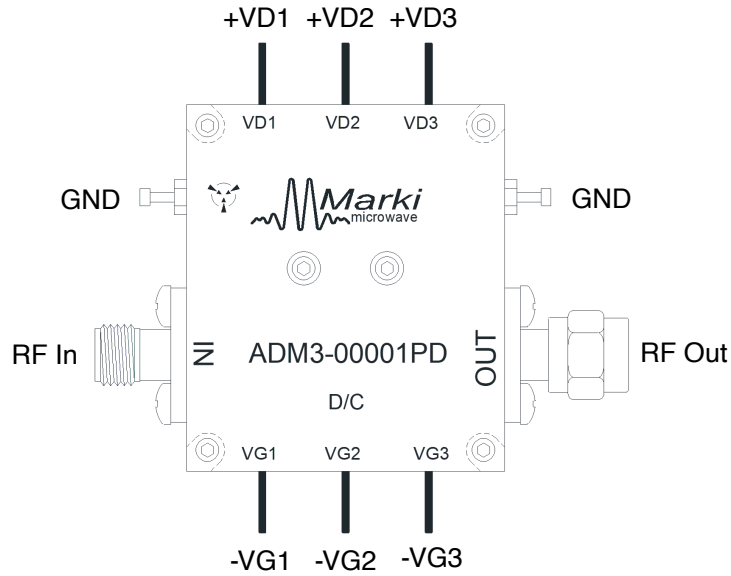
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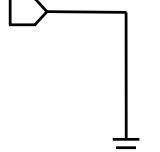
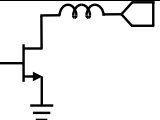
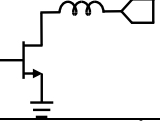
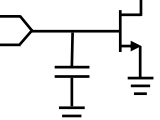
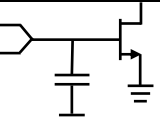
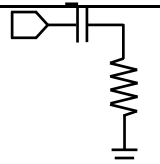
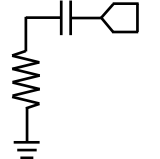
### Port Configuration and Functions

#### Port Diagram

A port diagram of the ADM3-00001PD is shown below.



**Port Functions**

Port	Function	Connector Type	Description	Equivalent Circuit for Package
GND	Ground	-	A single or both GND lugs must be connected to a DC/RF ground potential with high thermal and electrical conductivity. Ensure that the ground voltage is a common reference potential to all DC power supplies.	
P1, P2	Vd1, Vd2	-	P1 and P2 are the positive DC voltage supply pins for the drains on the 1st and 2nd stage amplifiers, recommended +5V. Vg1/Vg2 must be applied to P4/P5 prior to application of Vd1/Vd2 on P1/P2!	
P3	Vd3	-	P3 is the positive DC voltage supply pin for the drain on the 3rd stage amplifier, recommended +7V. Vg3 must be applied to P6 prior to application of Vd3 on P3!	
P4, P5	Vg1, Vg2	-	P4 and P5 are the negative DC voltage bias pins for the gates on 1st and 2nd stage amplifiers, recommended 0V. Must be applied prior to application of Vd1/Vd2 on P1/P2!	
P6	Vg3	-	P6 is the negative DC voltage bias pin for the gate on the 3rd stage amplifier, recommended -0.3V. Must be applied prior to application of Vd3 on P3!	
RF In	RF Input	2.92F	The RF input port of the amplifier is matched to 50Ω and has built-in DC blocking capacitors.	
RF Out	RF Output	2.92M	The RF output port of the amplifier is matched to 50Ω and has built-in DC blocking capacitors.	

### Specifications

#### Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If these limits are exceeded, the device may become inoperable or have a reduced lifetime. Reliability limits are individual, instantaneous catastrophic limits only. Functional operation limits are indicated below. Operation of the device at multiple absolute maximum limits or for extended periods at a single limit can cause degradation and damage to the device.

Parameter	Maximum Rating	Unit
Maximum Operating Temperature	55	°C
Maximum Storage Temperature	125	°C
Minimum Operating Temperature	-40	°C
Minimum Storage Temperature	-55	°C
P1 & P2 Drain Supply Voltage (Vd1, Vd2)	7	V
P1 & P2 Positive Bias Current (Id1, Id2)	150	mA
P3 Drain Supply Voltage (Vd3)	8	V
P3 Positive Bias Current (Id3)	230	mA
P4 & P5 Gate Bias Voltage (Vg1, Vg2)	0	V
P4, P5, P6 Gate Bias Current (Ig1, Ig2, Ig3)	0.5	mA
P6 Gate Bias Voltage (Vg3)	0	V
RF Input Power	-5	dBm
θJC, Junction to Ambient Thermal Resistance	10	°C/W

#### Package Information

Parameter	Details	Rating
Weight	Package name: PD	41g
Dimensions	-	33.02 x 38.10 mm

#### Recommended Operating Conditions

The Recommended Operating Conditions indicate the limits, inside which the device should be operated, to guarantee the performance given in Electrical Specifications.

Parameter	Min	Nominal	Max	Unit
Ambient Temperature	-40	25	55	°C
Gate DC Voltage (Vg3)	-0.5	-0.3	0	V
Gate DC Current (Ig3)	-	0	0.1	mA
Power Supply DC Current (Id3)	-	100	220	mA
Gate DC Voltage (Vg1, Vg2)	-0.5	-0.3	0	V
Gate DC Current (Ig1, Ig2)	-	0	0.1	mA
Input Power for Saturation	-	-10	-5.5	dBm
Power Supply DC Voltage (Vd3)	3	7	7.5	V
Power Supply DC Current (Id1, Id2) <sup>1</sup>	-	120	140	mA
Power Supply DC Voltage (Vd1, Vd2)	3	5	6.5	V

<sup>[1]</sup> Recommended operating current conditions without RF input applied.

#### Sequencing Requirements

Supply pin sequencing is required to power up or power down the amplifier. The amplifier must have an output load connected during operation.

Turn-on:

1. Ensure RF Out Port is connected to load.
2. Apply -0.3V to port P4 (Vg1) and port P5 (Vg2) and apply -0.3V to port P6 (Vg3).
  - a. Gate bias pins can be applied simultaneously.
3. Apply 5V to port P1 (Vd1) and port P2 (Vd2) and apply 7V to port P3 (Vd3).
  - a. Drain bias pins can be applied simultaneously.
4. Apply RF power to RF In Port.

Turn-off:

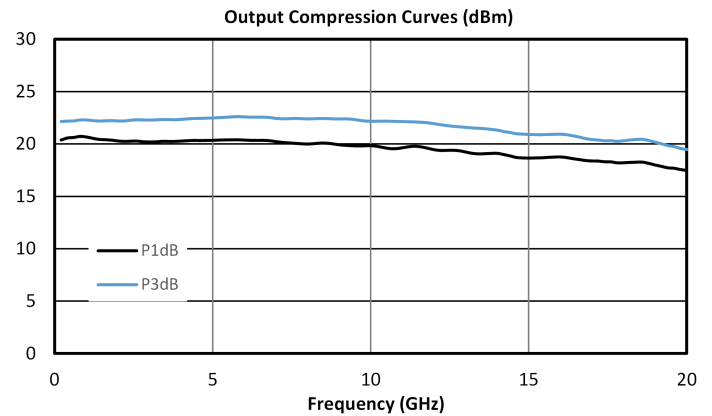
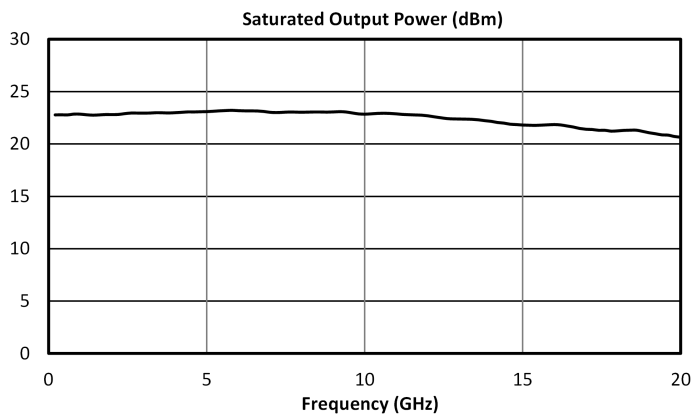
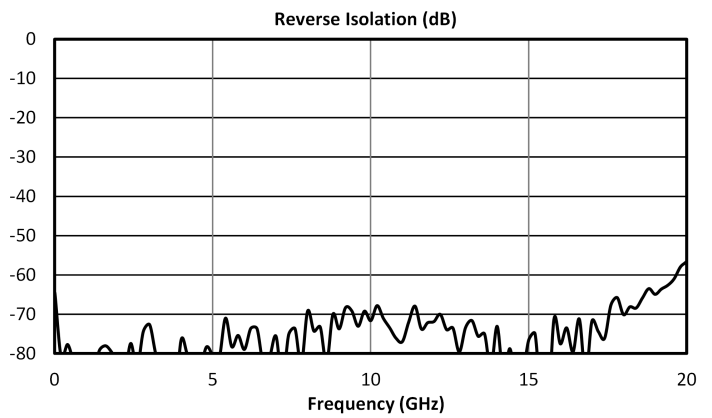
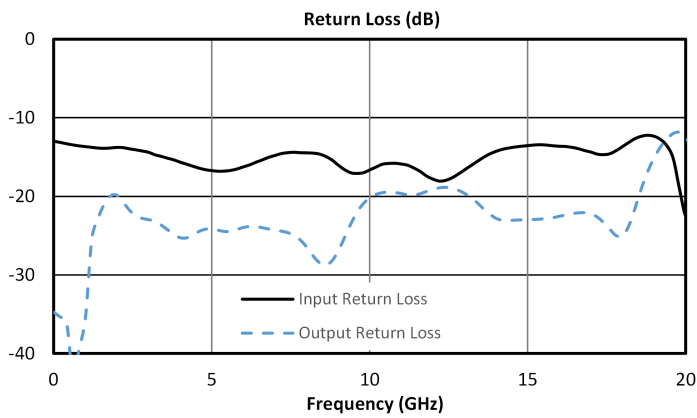
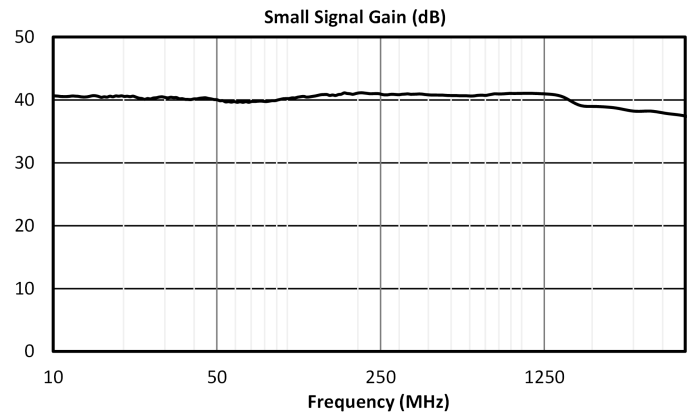
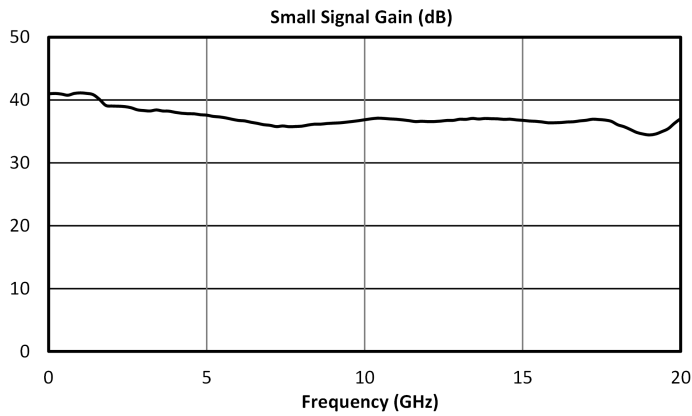
**Electrical Specifications**

Electrical specifications apply at Vd1=Vd2=5V, Vd3=7V, Vg1=Vg2=0V, Vg3=-0.3V in a 50Ω system at TA=+25° unless otherwise specified. Min and Max limits apply only to our connectorized units and are guaranteed at TA=+25°C

Parameter	Test Conditions	Minimum Frequency (GHz)	Maximum Frequency (GHz)	Min	Typ	Max	Unit
Input IP3	Characterization Bias, Pin = -40 dBm per tone, 10 MHz tone spacing	0.0003	18	-	-6	-	dBm
Input Power for Saturation	Characterization Bias	0.0003	18	-	-10	-	dBm
Input Return Loss	Vd1, Vd2 = 5V Vd3 = 7 V Vg1, Vg2 = 0V Vg3 = -0.3 V Pin = -40 dBm	0.0003	18	-	15	-	dB
Noise Figure	Vd1, Vd2 = 5V Vd3 = 7 V Vg1, Vg2 = 0V Vg3 = -0.3 V Pin = -40 dBm	0.0003	18	-	5	-	dB
Output IP3	Characterization Bias, Pin = -40 dBm per tone, 10 MHz tone spacing	0.0003	18	-	31	-	dBm
Output P1dB	Characterization Bias	0.0003	18	-	19.5	-	dBm
Output Power	Characterization Bias, Pin = -5 dBm	0.0003	18	18	23	-	dBm
Output Return Loss	Vd1, Vd2 = 5V Vd3 = 7 V Vg1, Vg2 = 0V Vg3 = -0.3 V Pin = -40 dBm	0.0003	18	-	23	-	dB
Reverse Isolation	Vd1, Vd2 = 5V Vd3 = 7 V Vg1, Vg2 = 0V Vg3 = -0.3 V Pin = -40 dBm	0.0003	18	-	75	-	dB
Rise Time	Characterization Bias, 10 MHz, 0.15Vpp square wave input	0.0003	18	-	44	-	ps
Small Signal Gain	Vd1, Vd2 = 5V Vd3 = 7 V Vg1, Vg2 = 0V Vg3 = -0.3 V Pin = -40 dBm	0.0003	18	32	37	-	dB

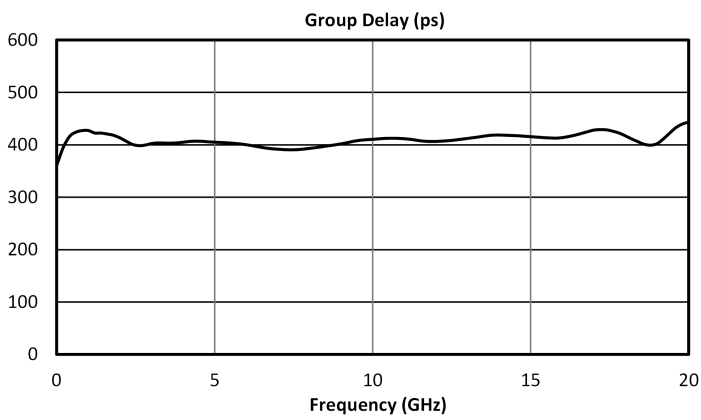
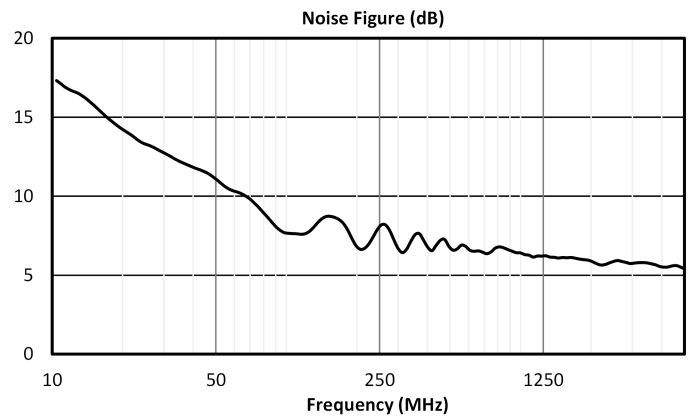
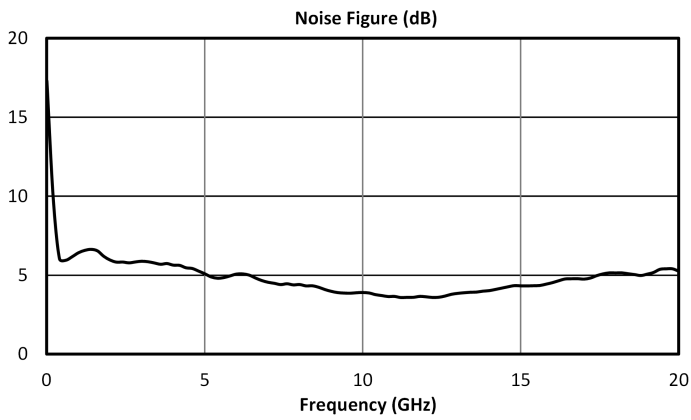
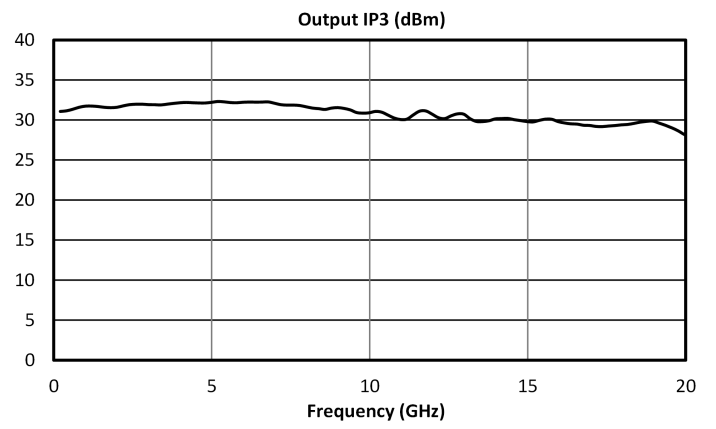
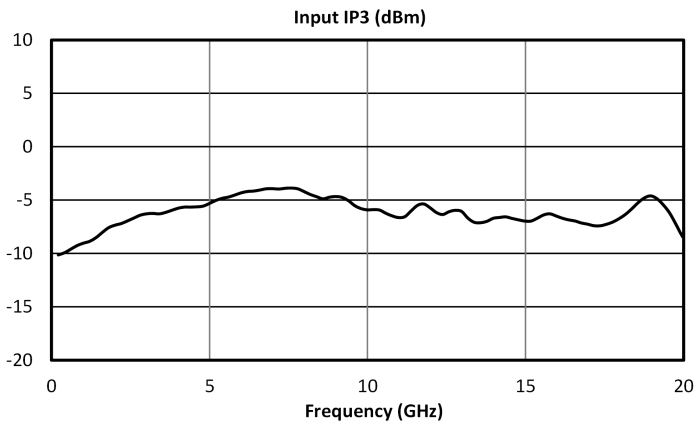
### Typical Performance Plots

Typical performance is characterized  $V_{d1}=V_{d2}=5V$ ,  $V_{d3}=7V$ ,  $V_{g1}=V_{g2}=0V$ ,  $V_{g3}=-0.3V$  in a  $50\Omega$  system at  $T_A=+25^\circ C$ .



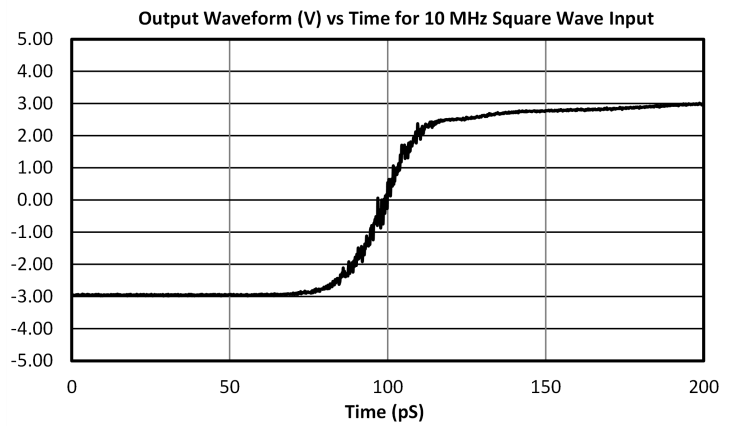
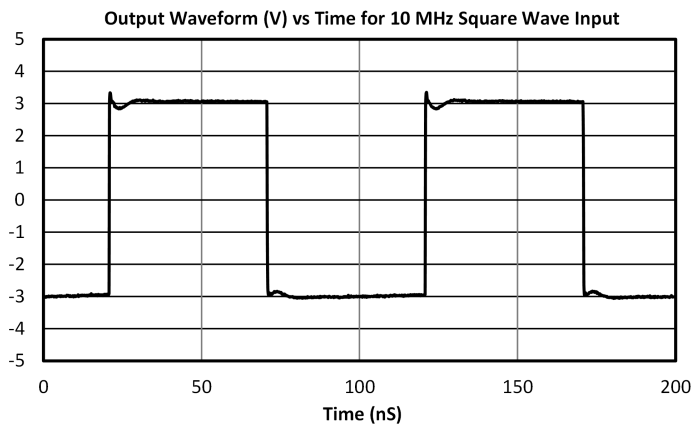
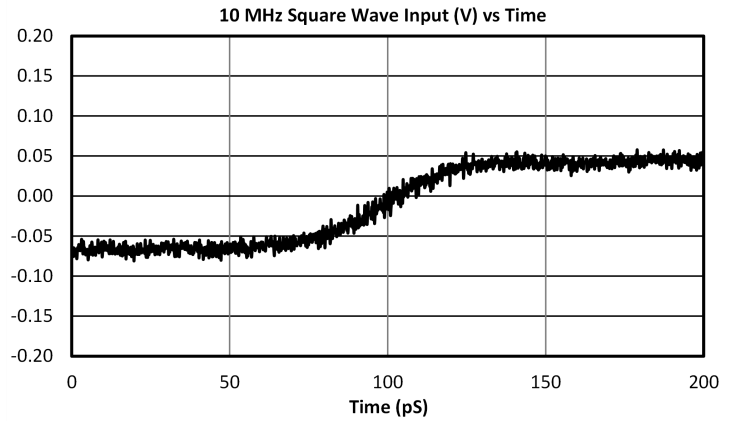
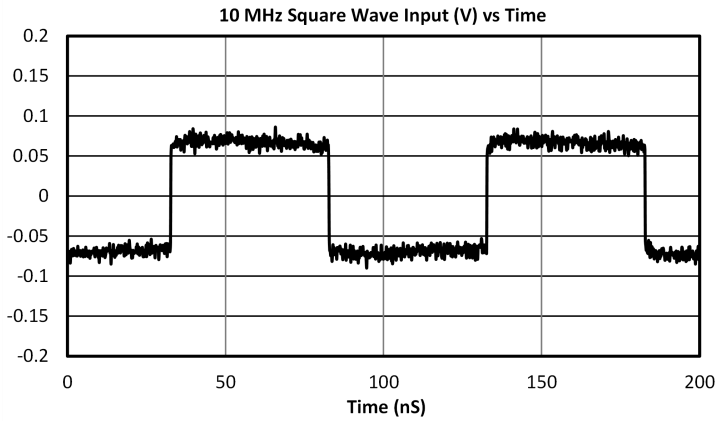
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**Time Domain Plots**

Typical performance is characterized at  $V_{d1}=V_{d2}=5V$ ,  $V_{d3}=7V$ ,  $V_{g1}=V_{g2}=0V$ ,  $V_{g3}=-0.3V$  in a  $50\Omega$  system at  $T_A=+25^\circ C$ .



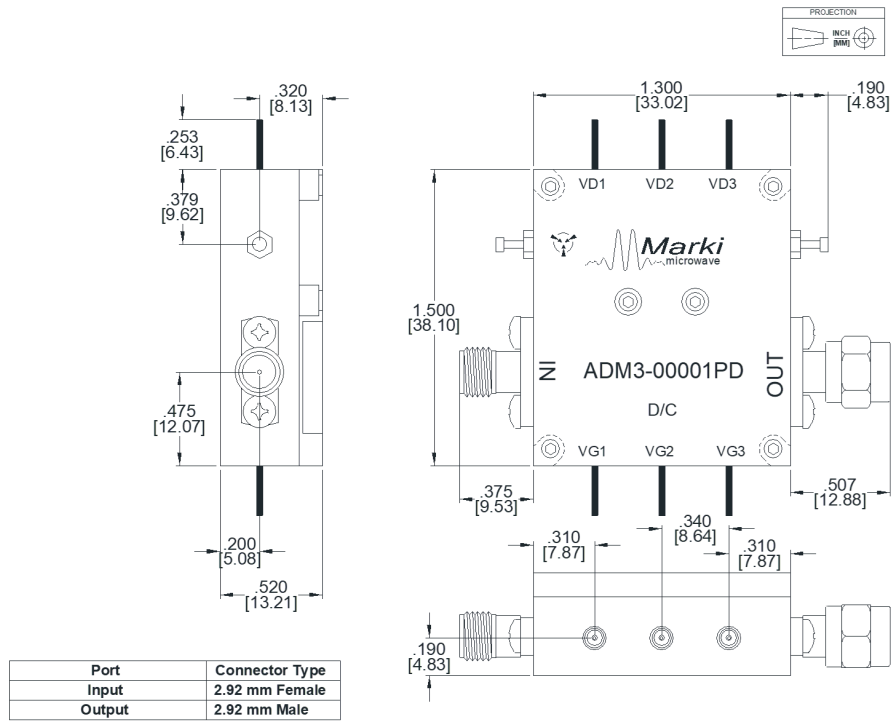
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## Mechanical Data

### Outline Drawing

Download : [Outline 3D Drawing](#) | [Outline 3D STP](#)



### Package Notes:

- 1) All measurements are typical.
- 2) Ground lug and bias pins are solderable.

## Notes

The ADM3-00001PD is for use in a controlled laboratory environment and is not suitable for use in high-reliability applications.

Module may be catastrophically damaged by heat. Special care must be taken to maintain operating temperature within limits.

Heat sinking is recommended to maintain proper operating temperature of the amplifier.

The amplifier may be catastrophically damaged by incorrect sequencing or disruption of the negative supply voltage. Always sequence according to Sequencing Requirements.

Operation of the amplifier without a load or with excessive output reflections can catastrophically damage the module.

Care must be taken to reduce or eliminate ESD discharge in the test environment.

Users must rigidly adhere to Absolute Maximum Ratings and Sequencing Requirements to prevent catastrophic failure.

Care must be taken to prevent damage due to excessive DC current, overheating, ESD, and damage due to large output reflections.

Care must be taken to avoid exceeding negative gate current rating listed in Absolute Maximum Ratings to prevent catastrophic failure.

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