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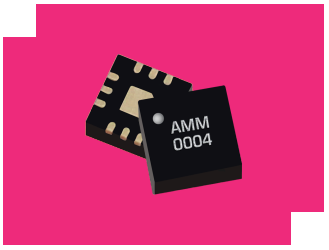
AMM-9859PSM

2 - 20 GHz Wideband Low Noise Amplifier

DEVICE OVERVIEW

General Description

The AMM-9859PSM is a wideband low noise amplifier capable of providing 15 dB gain and +28 dBm OIP3 with a low 1.9 dB typical noise figure. The AMM-9859PSM is an ideal linear signal amplifier for applications requiring low power consumption and small form-factors. This amplifier has exceptionally flat response across its entire operating bandwidth.



Download s-parameters here

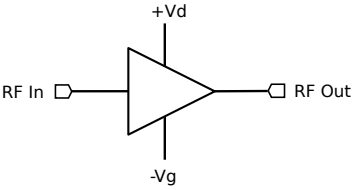
Features

- Broadband 2 to 20GHz Operation
- Low Noise Figure
- Exceptionally Flat RF Performance Across Frequency
- Excellent Return Losses

Applications

- Communication Systems
- Test and Measurement Equipment
- Satellite Communications
- Electronic Warfare

Functional Block Diagram



Part Ordering Options

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
AMM-9859PSM	2 - 20 GHz Wideband Low Noise Amplifier	QFN	RoHS REACH	Released	EAR99
EVB-AMM-9859P	Evaluation Board, AMM-9859PSM Wideband Low Noise Amplifier	-	REACH RoHS	Released	-

Table Of Contents

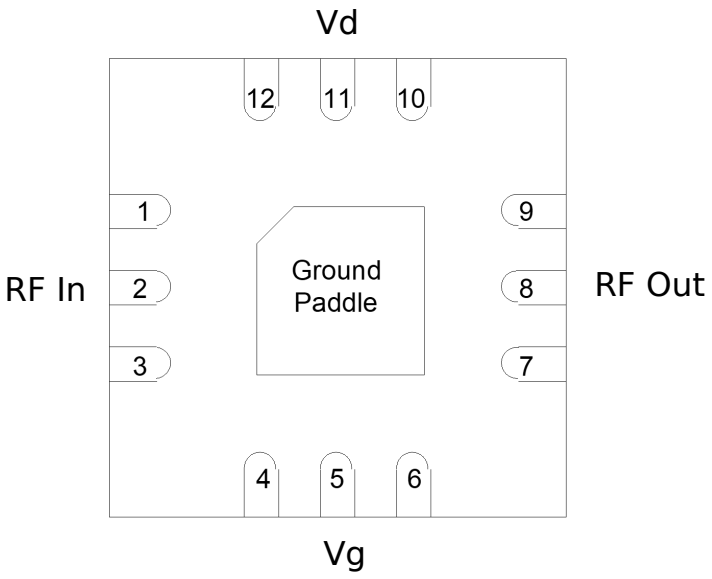
Revision History

Revision Code	Revision Date	Comment
-	2025-03-19	AMM-9859PSM
A	2026-02-13	MTTF Table Added.

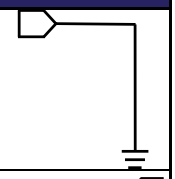
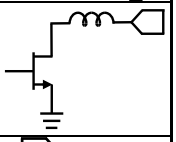
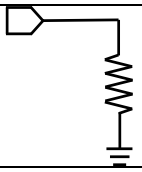
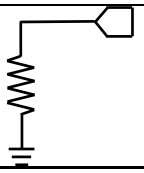
Port Configuration and Functions

Port Diagram

A port diagram of the AMM-9859PSM is shown below.



Port Functions

Port	Function	Description	DC Equivalent Circuit
Paddle	Ground	DC and RF Ground are provided through the QFN paddle. The paddle should be attached to a DC/RF ground with high thermal and electrical conductivity.	
Pin 11	Vd	This is the positive DC supply voltage for the amplifier IC. This pin is nominally set to +4V. This part requires an off-chip bypass capacitor of 0.1uF installed at this pin as close to the IC as possible. See applications circuit.	
Pin 2	RF Input	This is the amplifiers RF input port. This port is internally matched to 50 Ohms and is internally DC shorted to GND. This pin may be left floating if no DC is present on the line but should be DC blocked otherwise.	
Pin 5	Vg	This is the negative DC bias voltage for the amplifier IC. The voltage at this pin controls the current draw Id of the part. Higher voltage results in higher current. For normal operation, the voltage at this pin is adjusted to produce an Id of 32mA when Vd=4V. This part requires an off-chip bypass capacitor in series with a 10 Ohm resistor installed at this pin as close to the IC as possible. See applications circuit.	
Pin 8	RF Output	This is the amplifiers RF output port. This port is internally matched to 50 Ohms and is internally DC shorted to GND. This pin may be left floating if no DC is present on the line but should be DC blocked otherwise.	
Pins 1,3,4,6,7,9,10 and 12	Non-connect (NC)	These pins are not internally connected. Datasheet performance is measured with these pins connected to ground.	-

Specifications

Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If any one of these limits are exceeded, the device may become inoperable or have a reduced lifetime. Reliability limits are individual, instantaneous catastrophic limits only. Functional operation limits are indicated below. Operation of the device at multiple absolute maximum limits or for extended periods at a single limit can cause degradation and damage to the device.

Parameter	Maximum Rating	Unit
Drain Current (Id) (No RF Applied)	84	mA
Maximum Operating Temperature for MTTF > 1E6 hours	85	°C
Maximum Storage Temperature	125	°C
Minimum Operating Temperature for MTTF > 1E6 hours	-40	°C
Minimum Storage Temperature	-65	°C
Negative Bias Voltage	-2	V
Positive Drain Supply Voltage (Vd)	8	V
RF Input Power	10	dBm

FIT and MTTF Table

T (°C)	λ (TIF)	MTTF (hr)	MTTF (yr)
105	2,441.45	4.10E+05	47
85	310.48	3.22E+06	368
55	8.79	1.14E+08	12,992
25	0.12	8.24E+09	941,063

Package Information

Parameter	Details	Rating
Dimensions	-	3 x 3 mm
Moisture Sensitivity Level	-	MSL 1

Recommended Operating Conditions

The Recommended Operating Conditions indicate the limits, inside which the device should be operated, to guarantee the performance given in Electrical Specifications Operating outside these limits may not necessarily cause damage to the device, but the performance may degrade outside the limits of the electrical specifications. For limits, above which damage may occur, see Absolute Maximum Ratings.

Parameter	Min	Nominal	Max	Unit
Ambient Temperature	-40	25	85	°C
Positive DC Voltage (Vd)	4	4	4	V
Negative Bias Voltage (Vg)	-0.5	-0.4	-0.4	V
Positive DC Current (Id) (No RF Input)	17	32	32	mA

Sequencing Requirements

Turn-on Procedure:
1. Apply Vg (Pin 5)
2. Apply Vd (Pin 11)

Turn-off Procedure:
1. Turn off Vd (Pin 11)
2. Turn off Vg (Pin 5)

Note: RF input power can be injected at any moment in the bias sequencing procedure.

Electrical Specifications

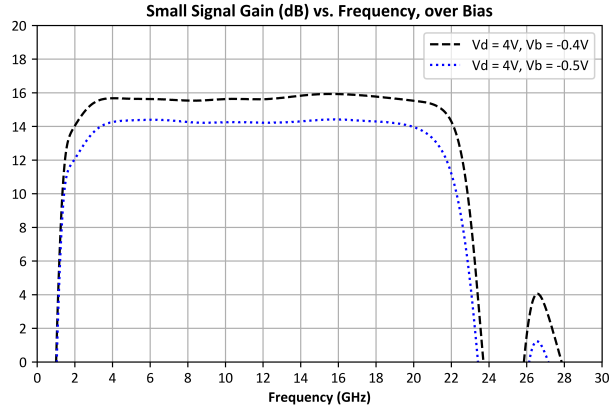
The electrical specifications apply at TA=+25°C in a 50Ω system. QFNs are 100% RF tested.

Parameter	Test Conditions	Minimum Frequency (GHz)	Maximum Frequency (GHz)	Min	Typ	Max	Unit
Small Signal Gain	Ta = 25°C, Input Power=-20.00 dBm, Vd1=4V, Vb1=-0.4V, Id1=32mA	0	20	-	15.5	-	dB
Input Return Loss	Ta = 25°C, Input Power=-20.00 dBm, Vd1=4V, Vb1=-0.4V, Id1=32mA	0	20	-	14	-	dB
Output Return Loss	Ta = 25°C, Input Power=-20.00 dBm, Vd1=4V, Vb1=-0.4V, Id1=32mA	0	20	-	16	-	dB
Reverse Isolation	Ta = 25°C, Input Power=-20.00 dBm, Vd1=4V, Vb1=-0.4V, Id1=32mA	0	20	-	21	-	dB
Noise Figure	Ta = 25°C, Input Power=-20.00 dBm, Vd1=4V, Vb1=-0.4V, Id1=32mA	2	20	-	1.9	-	dB
Output IP3	Ta = 25C, 4V/-0.4 bias, 20MHz tone spacing, Input Power = -10dBm	2	20	-	28	-	dBm
Output IP2	Ta = 25C, 4V/-0.4 bias, 20MHz tone spacing, Input Power = -10dBm	2	10	-	30	-	dBm
Output P1dB	Ta = 25°C, Vd1=4V, Vb1=-0.4V, Id1=32mA	2	20	-	14.5	-	dBm
Current Consumption [1]	4V/-0.4V bias, No RF Applied	-	-	-	32	-	mA
Saturated Output Power	-	2	15	-	19	-	dBm
Saturated Output Power	-	2	20	-	15	-	dBm

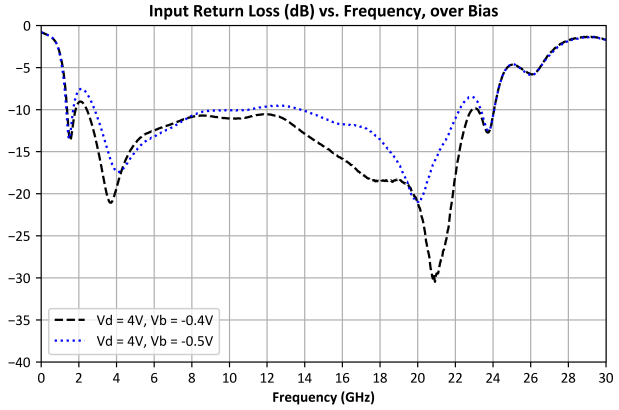
[1] Bias conditions for Id tested with no RF input power. Bias conditions presented as Vd/Vg.

Typical Performance Plots (vs Bias)

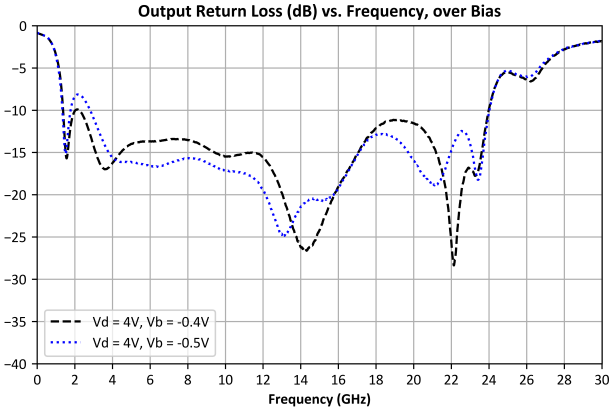
Small Signal Gain (dB) vs. Frequency, over Bias



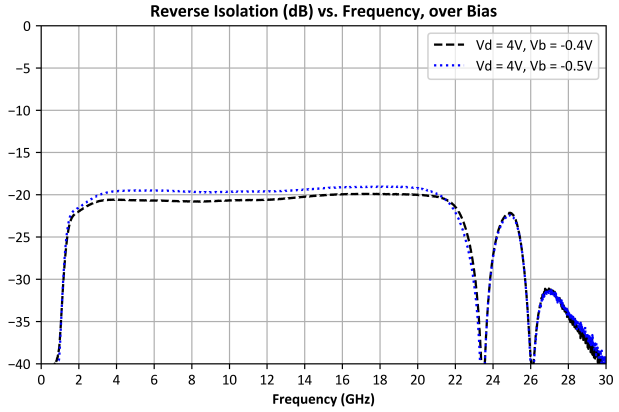
Input Return Loss (dB) vs. Frequency, over Bias



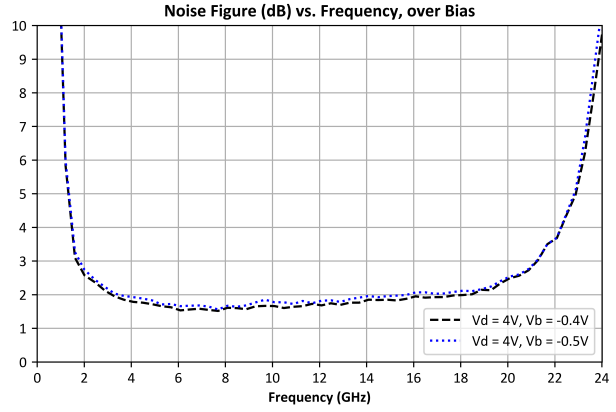
Output Return Loss (dB) vs. Frequency, over Bias



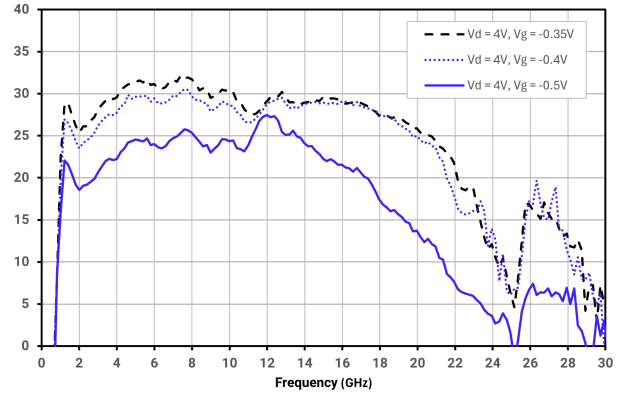
Reverse Isolation (dB) vs. Frequency, over Bias



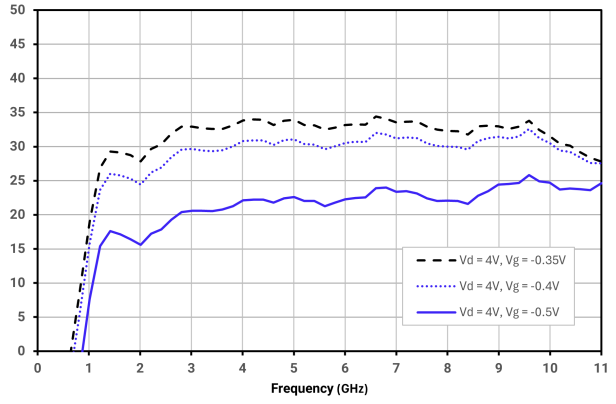
Noise Figure (dB) vs. Frequency, over Bias



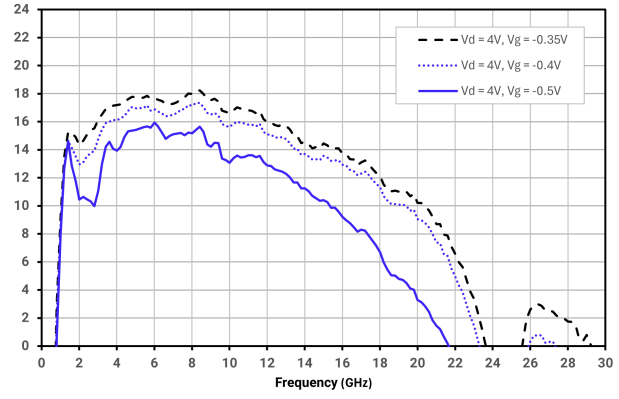
Output IP3 (dBm) vs. Frequency, over bias

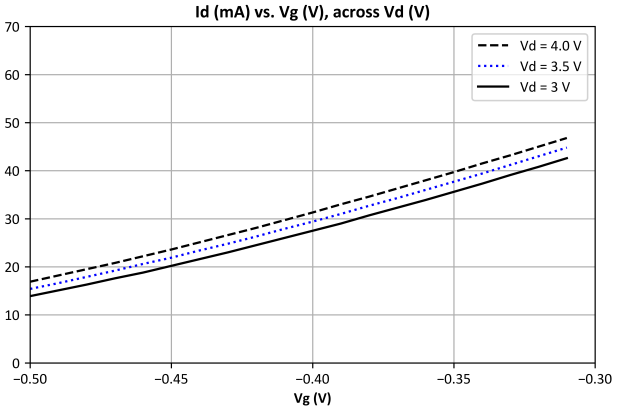


Output IP2 (dBm) vs. Frequency, over bias

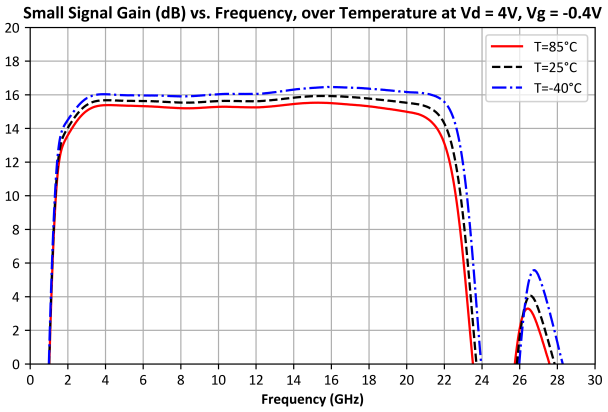


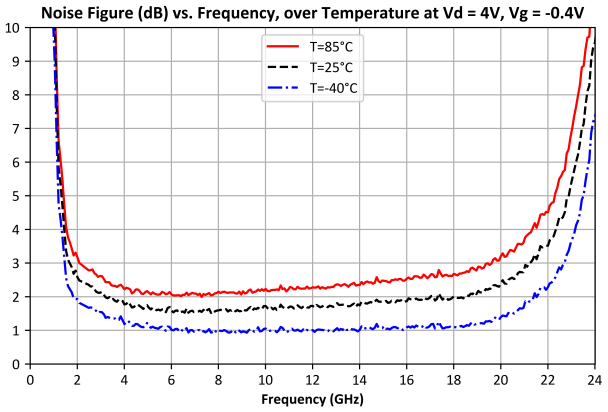
Output P1dB vs. Frequency, over bias



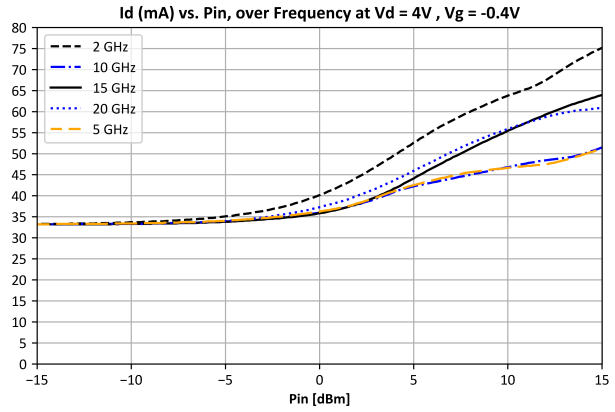


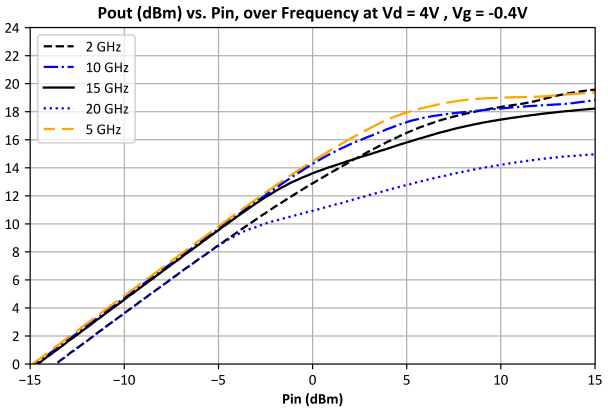
Typical Performance Plots (vs Temperature)

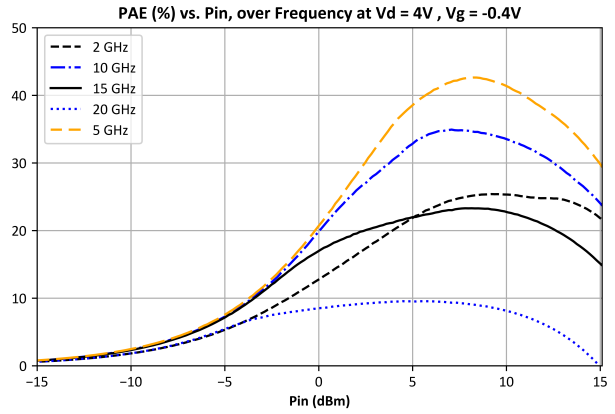




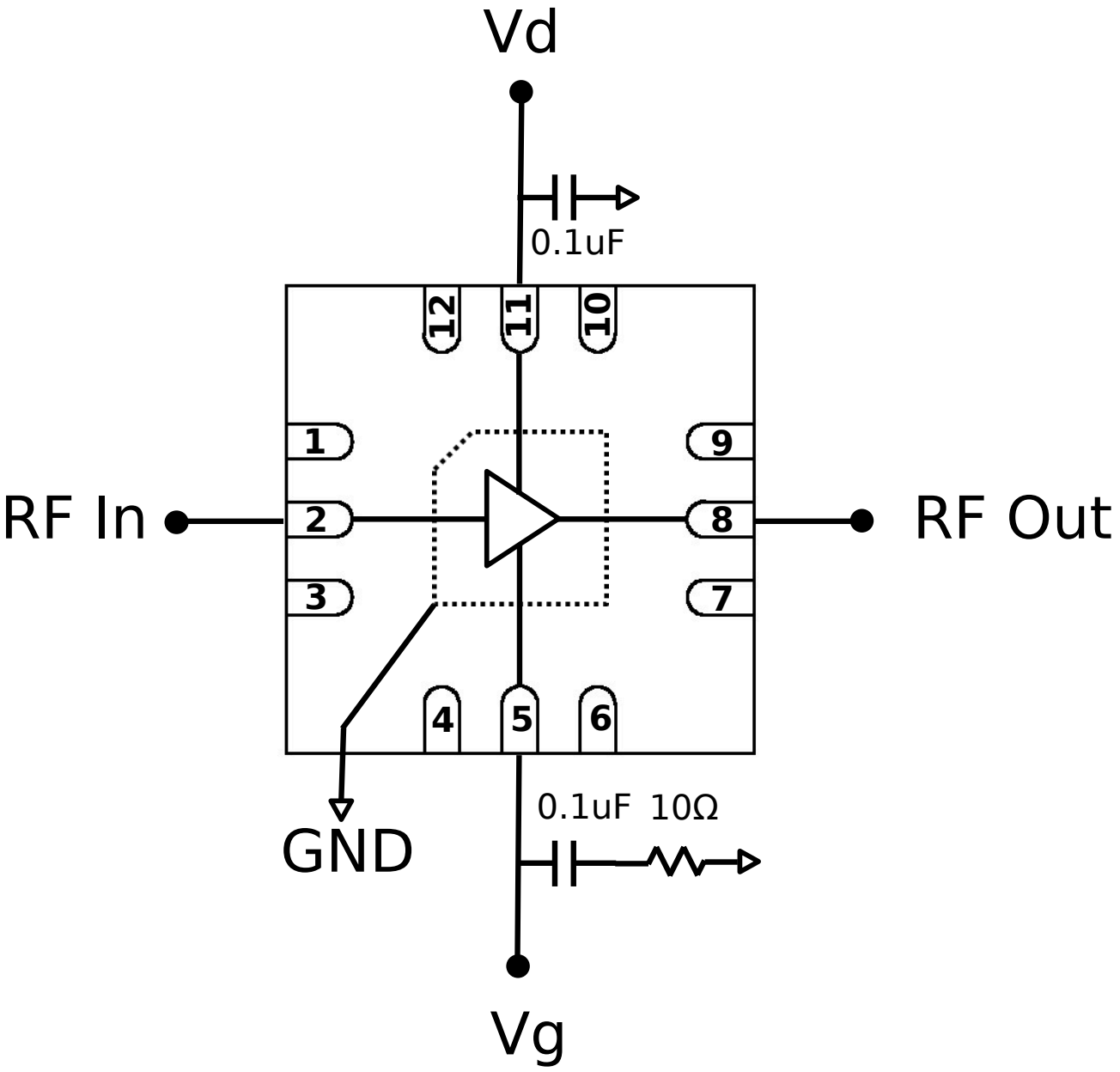
Typical Performance Plots (vs Input Power)







Application Circuit



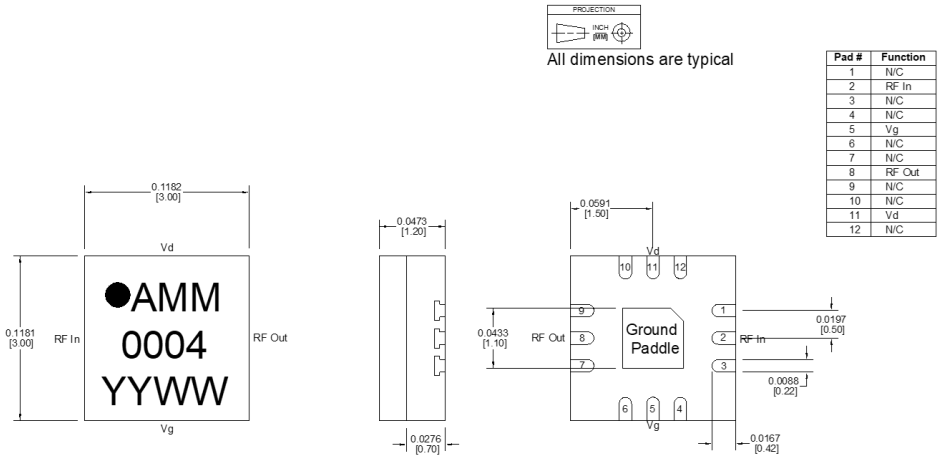
Application Circuit Description

Above is the recommended application circuit for the AMM-9859PSM. Multiple DC power supply bypassing capacitors are shown around the part. DC drain voltage is supplied to the amplifier across a 0.1uF bypass capacitor to the Vd pin. DC bias voltage is supplied to the Vg pin across a 0.1uF+10Ω bypass capacitor combination. The RF input and output ports are internally shorted to GND but can be left floating if no DC is present on the RF line. If DC is present, blocking capacitors are required at the input and output.

Mechanical Data

Outline Drawing

Download : Outline 2D Drawing



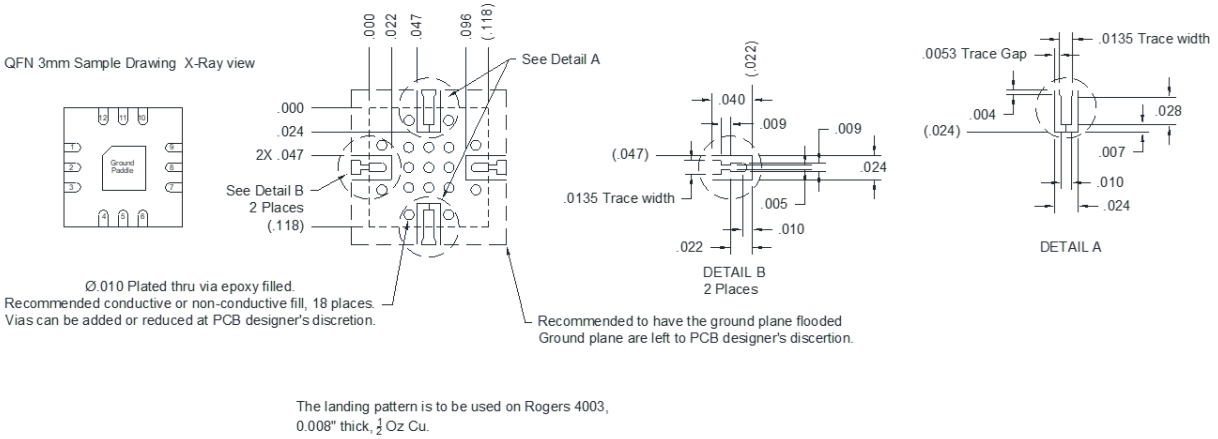
Pad #	Function
1	N/C
2	RF In
3	N/C
4	N/C
5	Vg
6	N/C
7	N/C
8	RF Out
9	N/C
10	N/C
11	Vd
12	N/C

Notes (unless otherwise specified):

1. Substrate material is LCP.
2. I/O Leads and Die Paddle are 0.05 micron Au over 0.02 microns Pd over 0.5 microns Ni.
3. All unconnected pins should be connected to PCB RF ground.

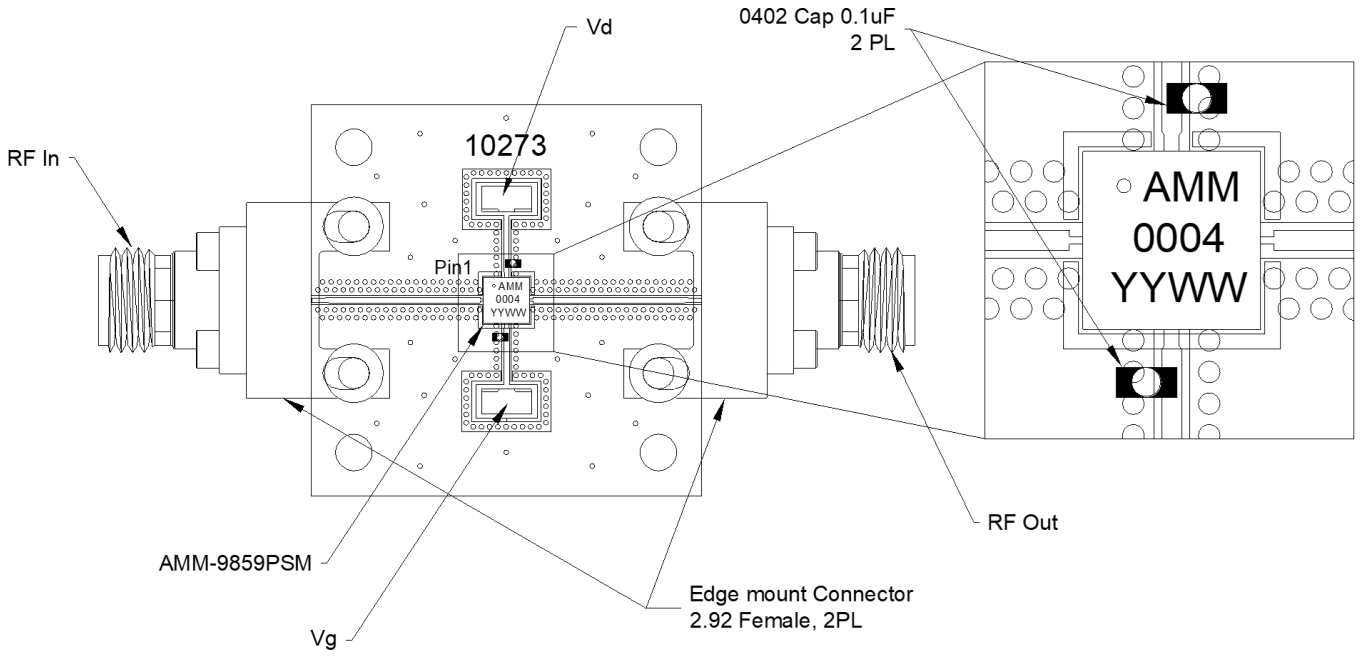
Footprint Image

Download : Footprint Drawing



The landing pattern is to be used on Rogers 4003,
0.008" thick, $\frac{1}{2}$ Oz Cu.

Evaluation Board - Outline Drawing



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