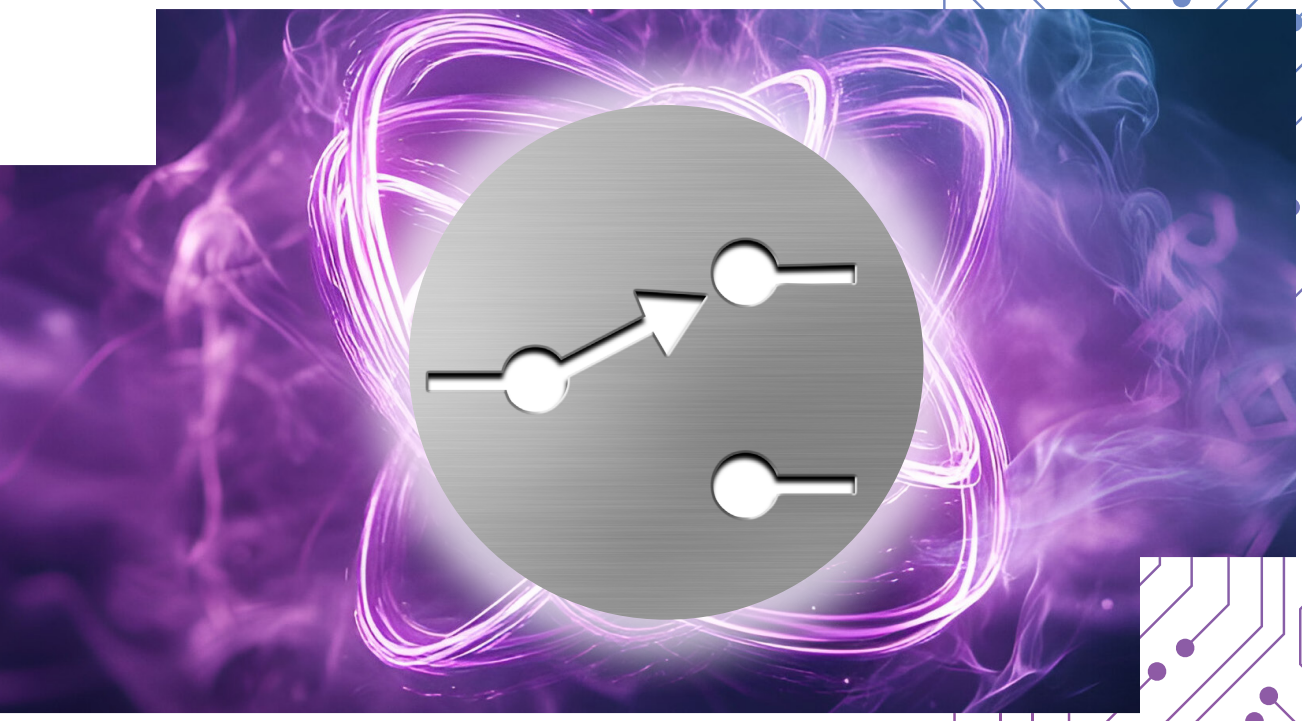
Marki microwave

PRIMER

Switch Basics



A Tutorial for RF and Microwave Switches

By: Del Pierson and Cameron Hill

RF and microwave switches route signals to different transmission paths without needing to disconnect a system. This functionality is key to a variety of applications and industries, such as signal routing across antenna ports, test and measurement equipment, and frequency-agile front ends. In concept, switching is straightforward- it is in a binary position of "ON" or "OFF". However, high performance RF switching is a complicated process that can be accomplished through a variety of technologies. This Switch Primer focuses on the Marki Microwave® metal-oxide semiconductor field-effect transistor (MOSFET) silicon on insulator (SOI) products. It covers the fundamental operating principles of MOSFET SOI switches, the evolution of switches, key performance parameters, hot-switching, FastSwitch™ technology, and shows why Marki Microwave's products are market leaders in high performance switch products.

I. WHAT IS A SWITCH?

RF switches are multiport devices that enable engineers to route signals to different paths without physically breaking a signal chain. They are used in every industry that employs RF. There are several categories of switch configurations:

- Single pole, double throw (SPDT): one input signal to two output paths
- Single pole, multiple throw (SPnT): one input signal to multiple output paths
- Multi pole, multi throw (mPnT): multiple inputs to multiple output paths.

Further, switches in the above configurations can be categorized into either:

- Reflective switches
- Absorptive switches

Reflective switches do not contain internal 50 Ω terminations on the unused RF ports, as demonstrated in **Figure 1**. Each unused port is terminated to ground through the small ON resistance of the FETs in the shunt path, or in an open circuit.

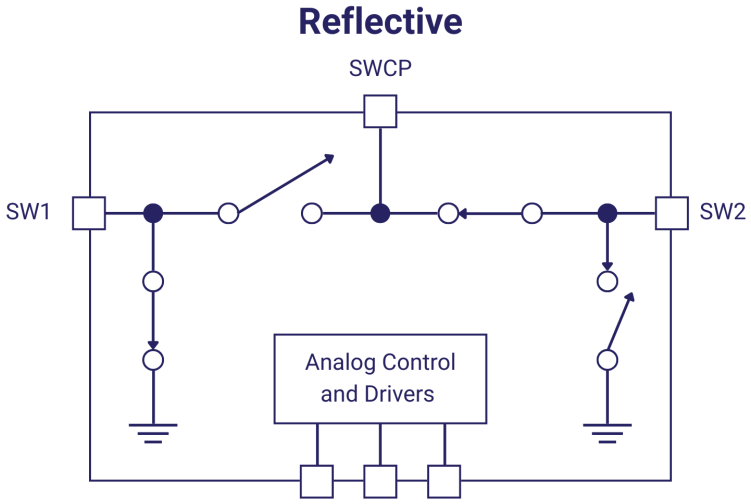


Fig. 1: *Schematic of a reflective switch.*

Alternatively, absorptive switches do contain internal 50 Ω resistive terminations on RF ports, as shown in **Figure 2**. Each unused port is terminated to ground through the ON resistance of shunt-path FETs in series with the resistive termination, presenting a matched load and minimizing reflected energy. In general, absorptive designs are preferred in systems sensitive to reflected power, such as cascaded amplifier chains, where a reflective switch can cause undesired interactions with the driving stage.

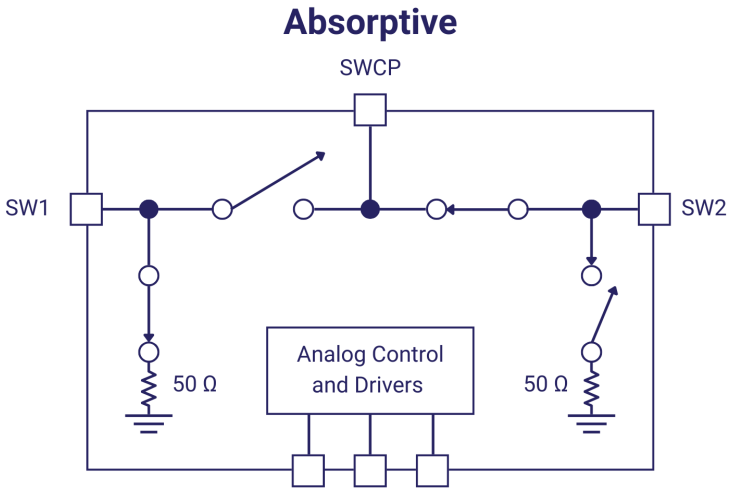


Fig. 2: *Schematic of an absorptive switch.*

Choosing a switch configuration is dependent on the needs of the system, and switches can be grouped into matrices to suit more complicated systems, such as software defined radios, or used in high volume, such as in phased arrays.

In addition to the different configurations, switches can be broken into different technologies, starting with electromechanical and solid state technologies. Electromechanical switches rely on moving mechanical contacts as their switching method, while solid state switches are based on semiconductor technology. Marki Microwave designs and produces solid state switches using MOSFET SOI technology, but it is worth examining the other technologies to understand why.

II. SWITCH TECHNOLOGIES

There are multiple technologies within the different switch types. Electromechanical switches include electromechanical relays and micro-electromechanical systems (MEMs), and solid state switches can use a variety of semiconductor technologies including PIN diodes, GaAs, GaN, bulk silicon, and SOI CMOS. **Table 1** examines the advantages and disadvantages between electromechanical and SOI CMOS switches. **Figure 3** shows a schematic of an electromechanical switch.

Category	SOI CMOS	E-M Relays	MEMs
Switching speed	Fast (ns)	Slow (ms)	Slow (ms)
Hot-switching	Robust to hot-switching	Sensitive	Sensitive
Lifetime	10 years typical, independent of switching events	Short and dependent on number of switching events	Short and dependent on number of switching events
Investment history	Robust commercial investment	Robust commercial investment	Limited commercial investment
Size	SWaP otimized	Very large	Large
Cost per switch	Low	High	Medium
Power handling at DC	Low	High	High
Loss	Low	Low	Low

Table 1: *SOI CMOS versus electromechanical relay and MEMs technology.*

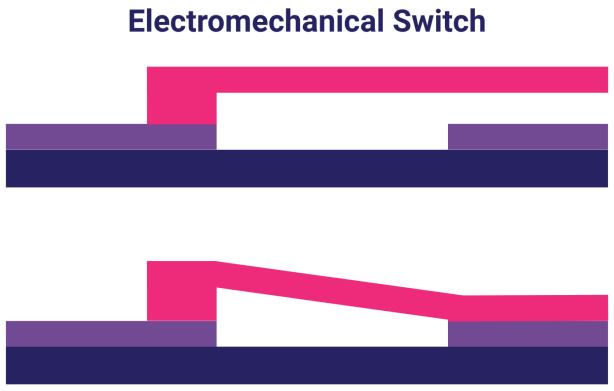


Fig. 3: *Schematic of an electromechanical switch.*

Mechanical switches predate semiconductors and still have appeal in test equipment and other applications that require very low loss and can pass DC signals. However, because the mechanical switches have moving parts, their reliability and switching time are the bottlenecks that exclude them from most communications, radar, and other wireless markets.

For high performance wireless systems, PIN diodes have historically dominated the market due to their high power handling, low loss, and fast switching. **Table 2** shows the attributes of SOI CMOS versus PIN diodes, and **Figure 4** shows the difference in schematics between the technologies. Notice how the PIN diode is a significantly more intricate, and therefore larger, circuit.

SOI CMOS	PIN Diode
Low DC power requirements	High DC power consumption
Simple biasing	Complex biasing schemes
Low video feed-through	Large video feed-through due to high voltage control circuit
Can be used for low frequencies	Low frequency cut-off
High process reliability	Process reliability concerns

Table 2: *SOI CMOS versus PIN diode technology.*

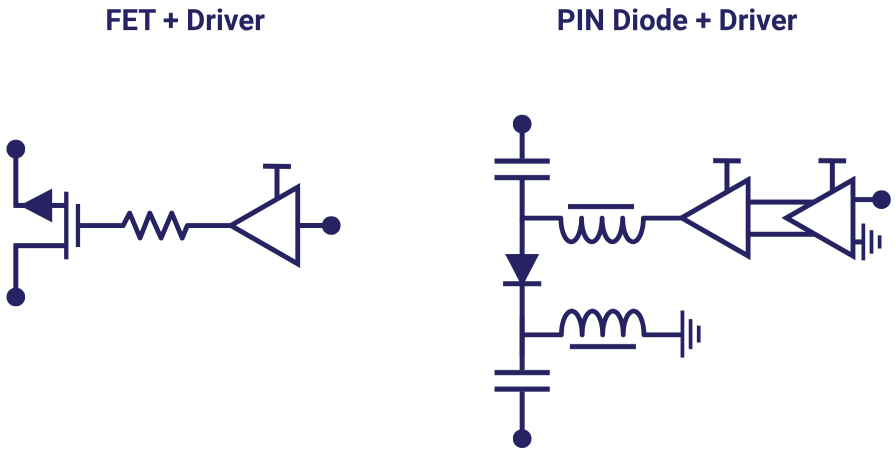


Fig. 4: *Schematic of a FET compared to a PIN diode.*

FETs are not confined to SOI alone; FETs can also be made from bulk silicon, GaAs, and GaN. **Table 3** outlines the pros and cons of SOI CMOS, GaAs, and GaN technology.

Category	SOI	Bulk CMOS	GaAS	GaN
Loss	Low	Moderate	High	High
Power handling	High	Low	Moderate	High
Switching time	Slow when designed for high power*	Fast	Fast	Fast
Settling time	Slow when designed for high power*	Fast	Long due to gate lag	Long due to gate lag
ESD robustness	High	Low	Intrinsically low but can be designed	Intrinsically low but can be designed
Process stability	High	High	Moderate	Low
Cost	Low	Low	Moderate	Expensive
Bias voltage	Low*	Low	Moderate	High and negative

Table 3: *SOI CMOS versus other semiconductor material switches.*
**without Marki FastSwitch™ technology*

SOI is the dominant technology for applications that require low cost and high performance and have relaxed switching time requirements, such as handset frontends and filter banks. For applications that do not allow the compromise on switching speed, such as radar and electronic warfare, PIN diodes have dominated, and GaN is an emerging technology that is gaining traction. However, with Marki Microwave's FastSwitch approach, the commercial scale that has driven SOI to dominance in handsets can be leveraged to yield very high performing switches in the aerospace and defense markets without compromise, as will be discussed later.

III. SWITCH METRICS

Like all RF devices, switches have many metrics, each of which are optimized for different systems. Measurable metrics for switches include insertion loss, isolation, power handling, linearity, switching time, settling time, and spurs. Much of the switch performance is dominated by the fundamental technology figure of merit, the $R_{on}C_{off}$ constant. $R_{on}C_{off}$ describes the ability of the device to have low loss and high isolation simultaneously, and is usually expressed in femtoseconds. **Figure 5** shows the change in the characteristics of the device with different bias as the FETs toggle between resistances and capacitances in the RF system. The next subsections will cover how this constant can impact the system.

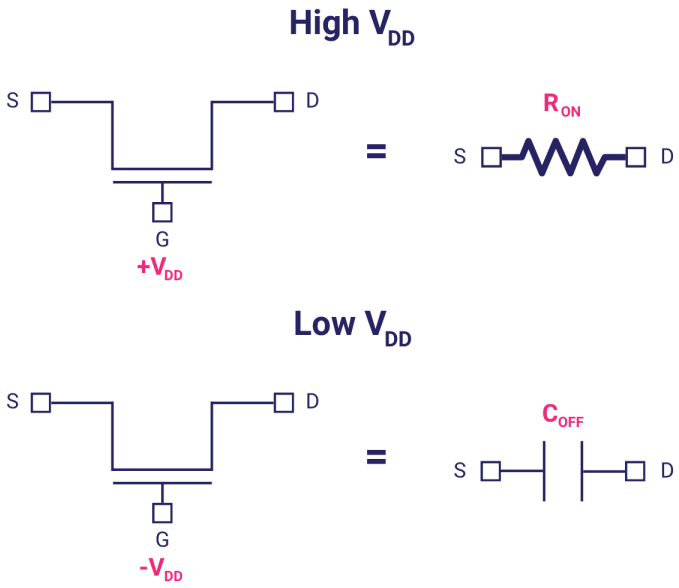


Fig. 5: *Schematic of a) high V_{DD} and b) low V_{DD}.*

Switch performance is measured by R_{ON}*C_{OFF}. R_{ON}, as previously defined, represents the transistor when it acts like a resistor in the switch's ON state. R_{ON} is inversely proportional to the width of the transistor. C_{OFF}, on the other hand, represents the transistor when it acts like a capacitor in the switch's OFF state. C_{OFF} is directly proportional to the transistor width.

In an ideal switch, R_{ON}*C_{OFF} is zero, so the signal is strong in the ON state and does not leak in the OFF state. However, like most electromagnetic parameters, ideal performance is unachievable in the real world. Therefore, the goal of switch designers is to minimize R_{ON} and C_{OFF} to extend bandwidth and improve insertion loss. Successive generations of SOI processes have progressively reduced R_{ON}*C_{OFF}, following a technology evolution from 500 nm node processes through 350 nm to 22 nm. At each node, designers can either reduce C_{OFF} while holding R_{ON} constant, or reduce R_{ON} while holding C_{OFF} constant, depending on the target application. **Figures 6a** and **6b** show these relationships.

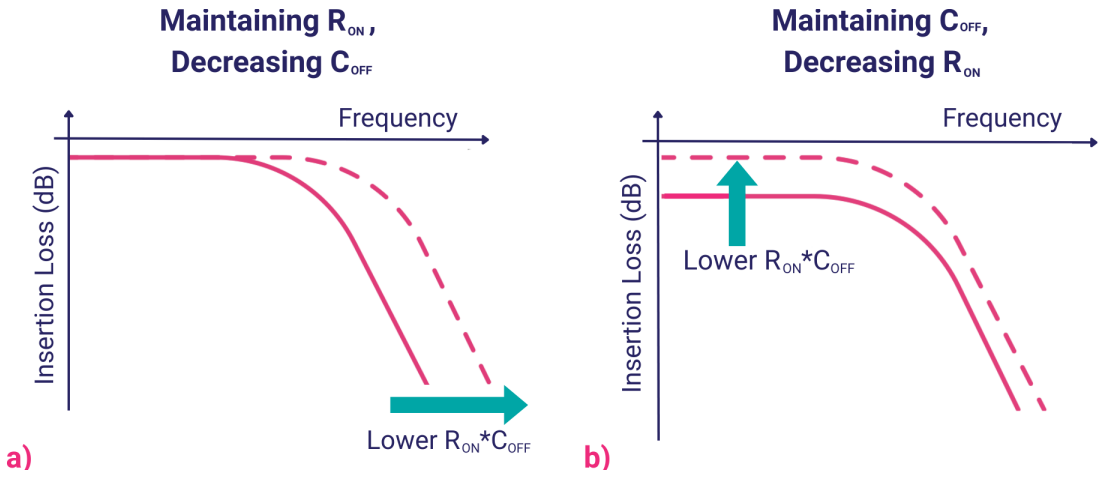


Fig. 6*: Impact of (a) maintaining R_{ON} and lowering C_{OFF} and (b) maintaining C_{OFF} and lowering R_{ON}.*

A. Insertion Loss

Insertion loss (IL) is the signal attenuation experienced on the "through" path of the switch in its ON state. In an ideal device, the FET would be purely resistive (R_{ON}), producing a flat, frequency-independent loss. In practice, in an SPDT switch, the OFF state device contributes substantial capacitance (C_{OFF}) to the other switching paths, creating an effective RC filter, as shown In **Figure 7**.

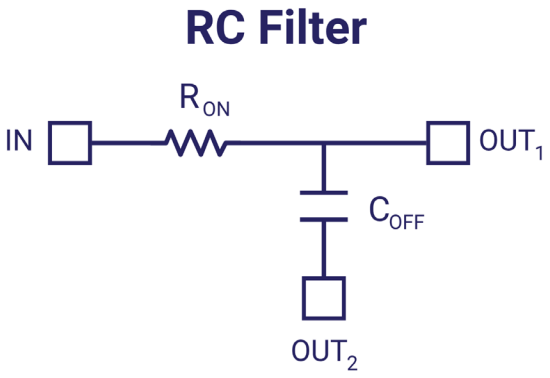


Fig. 7: *Parasitic shunt capacitance.*

As frequency increases, the impedance of C_{OFF} decreases, diverting more signal energy through the OFF path. Eventually, the ON path and OFF path present the same impedance, and toggling the switch no longer accomplishes any signal routing. This point is referred to as the cutoff frequency and is shown in **Equation 1**.

$$\omega_O = \frac{1}{(R_{ON} \times C_{OFF})} \quad (1)$$

Similar to increasing frequency, increasing the number of throws per switch degrades the insertion loss. This is because each additional OFF throw path adds a shunt capacitor in parallel with the ON path. As the number of throws increases, the total shunt capacitance grows, causing the frequency response to roll off faster (**Figures 8a and 8b**). This is a fundamental architectural trade-off: higher throw-count switches suffer greater high frequency insertion loss degradation.

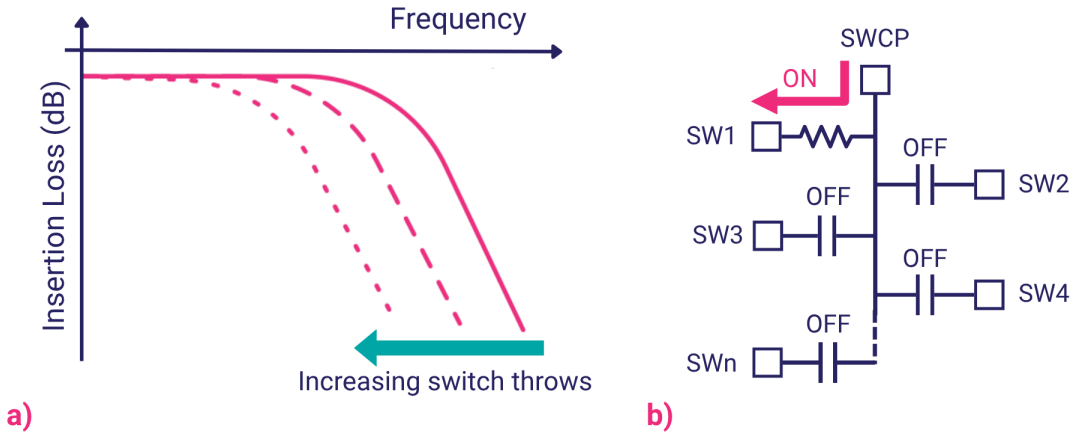


Fig. 8*: A (a) graph and (b) schematic of the performance impact of multi-throw switches.*

B. Isolation

Isolation quantifies how well a switch prevents signal leakage from the ON path to the OFF ports. Ideally, when the transistor is OFF, no RF signals propagate from one terminal to the other. This is typically true at low frequencies, however, at high frequencies, RF signals often leak from one terminal to another due to coupling on the chip, in the package, or on the evaluation board. With an OFF FET, the simplified isolation and graph is shown in **Figures 9a** and **9b**. To improve isolation, designers can terminate the switch with a lower resistance. Adding shunt FETs to the thru paths will lower the terminating resistance.

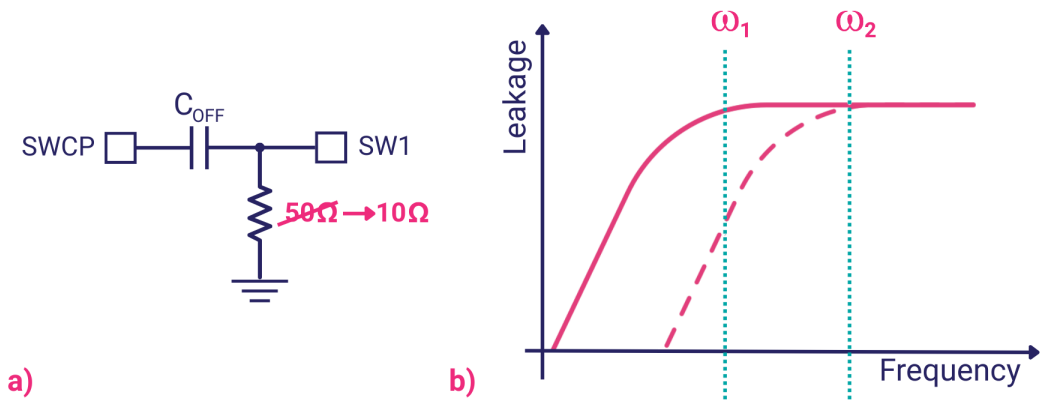


***Fig. 9**: Isolation circuit (a) schematic and (b) graph.*

Shunt FETs are biased OFF when their associated through path is ON, and ON (presenting a low-resistance path to ground) when the through path is OFF. This creates a lower-impedance shunt that attenuates leakage signals more effectively. However, added shunt FETs introduce a fundamental design trade-off: while improving isolation, they add capacitance to the ON path, degrading bandwidth in a manner similar to adding extra throws. Designers must balance the isolation requirement against acceptable bandwidth degradation. **Figure 10** shows the change in circuit when thru paths and shunt FETs are ON and OFF.

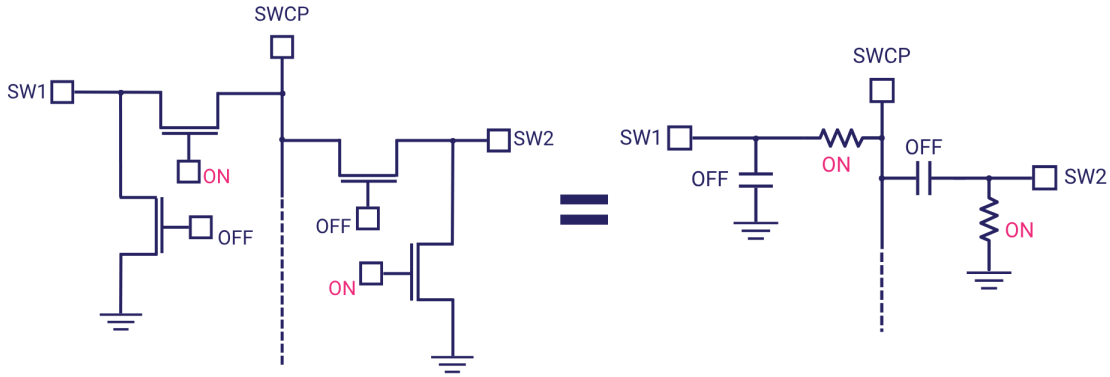


***Fig. 10**: Circuit equivalence when the thru path and shunt FETs are ON or OFF.*

C. Power Handling

A switch's power handling capability is determined by its ability to withstand peak voltage across the input port to ground (shunt switches) and the input port to all other ports (series switches). This peak voltage appears when RF power is applied to any input port (**Figure 11**).

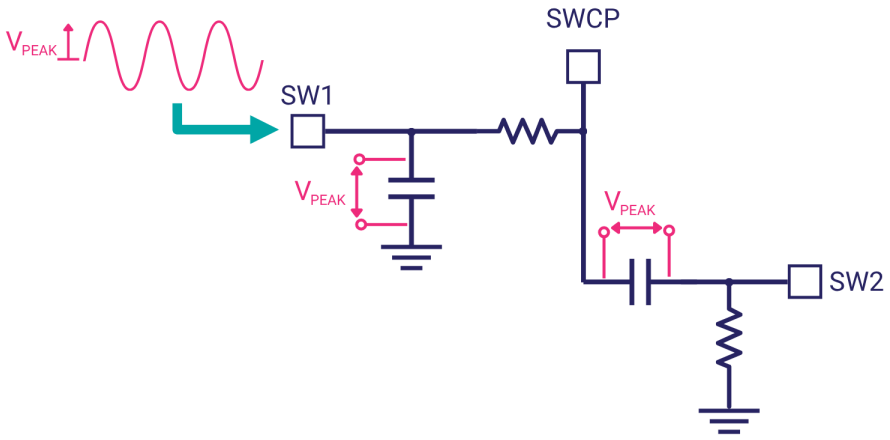


***Fig. 11**: Schematic of peak voltage across an SPDT with shunt devices at the two terminals.*

SOI, GaAs, and GaN have the advantage over bulk silicon in that they generally have high resistivity or isolating substrates. This keeps different FETs on the same die highly isolated, allowing each node of the FET to float at an arbitrary voltage. This key difference between bulk silicon and SOI is shown in **Figure 12**.

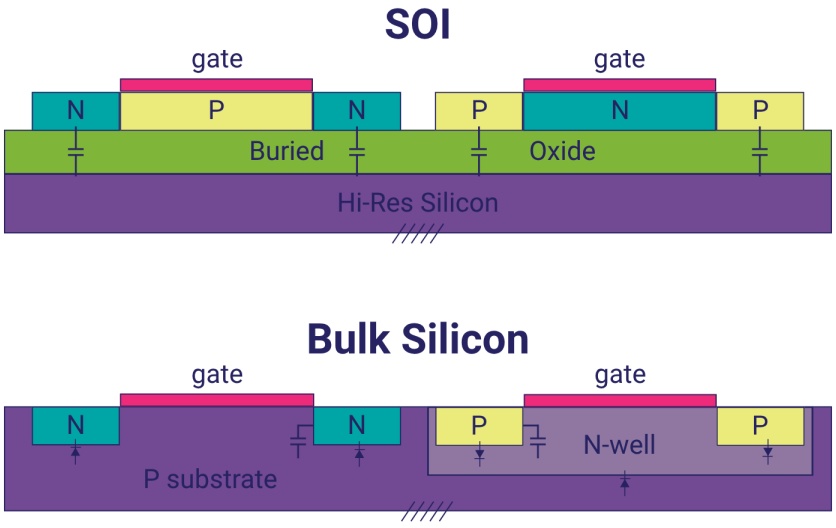


***Fig. 12**: Stack ups of SOI and bulk silicon technology where the buried oxide allows high isolation between different FETs in SOI, while the bulk silicon devices are not well isolated.*

A typical FET on an isolating substrate will be linearized by adding a large resistor to the gate to ensure that the gate maintains the appropriate bias through the entire phase of the RF signal, as shown in **Figure 13**.

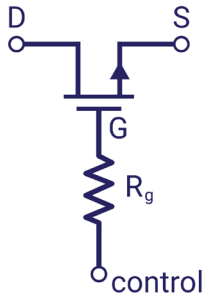


***Fig. 13**: Schematic of a linearized FET switch where R_g presents a large impedance compared to C_g, allowing the gate to swing in unison with the drain and source, and maintain linearity under exposure to a large RF signal.*

One benefit of SOI CMOS technology is the ability to stack FETs in series to improve power handling, also due to the isolating nature of the substrate. This is an effective method to increase power handling since the voltage across the FET stack is equally distributed between the individual devices. Therefore, doubling the FET stack height will double the voltage handling and quadruple the instantaneous power handling. However, R_g and C_g create a corner frequency, below which the gate no longer follows the RF signal and the switches become non-linear regardless of the stack height. R_g can always be increased to reduce the corner frequency; however, it comes at the cost of switching time. **Figure 14** demonstrates the distribution of voltage across the FET stack.

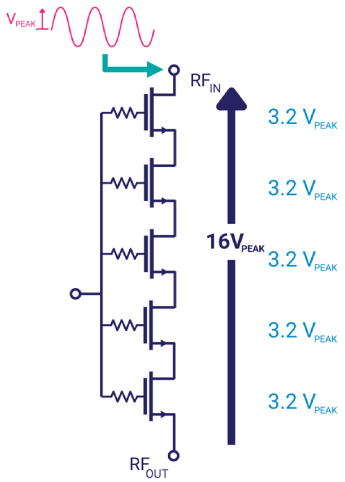


***Fig. 14**: Example of power distribution with low and high frequency FET stacking.*

Larger stacks of FETs do degrade the R_{on}*C_{off} product of the combined switch device. However, the R_{on}*C_{off} product starts at a point so much better than III-V semiconductors (GaN and GaAs), that even with the degradation that comes with higher breakdown voltage stacks, the FOM remains superior at >100 V peak, as shown in **Figure 15**. These types of designs are regularly used in the commercial world for antenna tuners that need to withstand very large VSWR values, and limiters that are used to protect sensitive receiving elements.

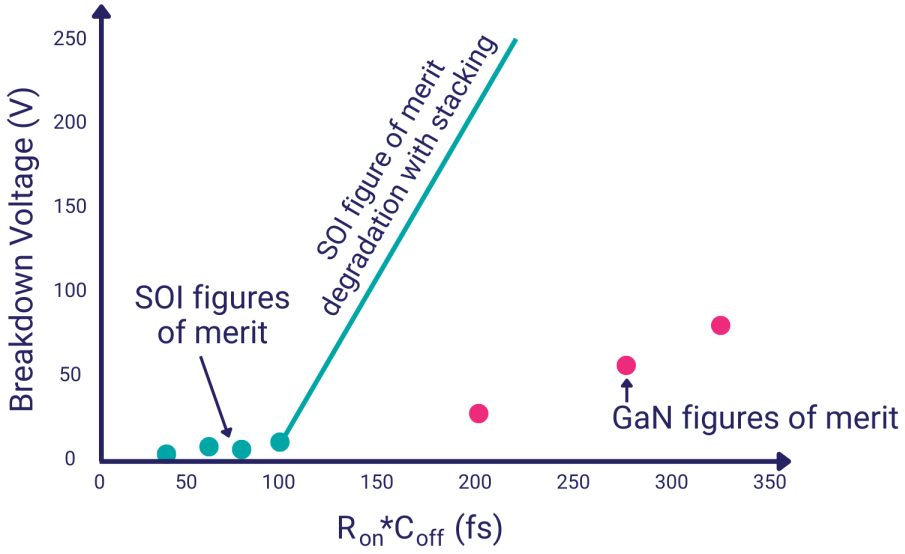


***Fig. 15**: Comparison of SOI and GaN figures of merit and the trend in FOM degradation with increasingly large SOI stacks.*

The key disadvantage of using exceedingly large, stacked SOI devices for high power is that the switching time increases exponentially as the length, width, and gate resistance must all be increased to achieve higher breakdown voltages. Compared to GaN switches, where only a few stacked devices are needed for very high breakdown voltages, SOI has historically had much slower switching times. With Marki's breakthrough with the FastSwitch™ architecture, this trade-off has largely been solved, allowing SOI to outperform GaN.

D. Linearity

Linearity of a switch differs from what most engineers think of in an amplifier or other active device. Since the FETs (or other devices) are biased deeply into either an ON or OFF state but have aggressive non-linear behavior when the voltages start to clip (breakdown), the difference between P1dB and IIP3 can be much greater than 10 dB, which is the "textbook" difference between the two linearity metrics. In other words, the switches can exhibit extremely linear behavior as long as they are not reaching device breakdown. It is common for switches in cellular handsets and test and measurement systems to have P1dBs in the range of 30 dB but IIP3s above 70 dBm. This is partially accomplished using SOI, which is intrinsically linear due to the minimal body diodes and other active parasitics that have been engineered out of the silicon. In SOI, the remaining factors that contribute to distortion are small changes in resistance across voltage swings, charges moving in the handle wafer of the SOI, and small changes to the OFF state conductivity as breakdown is approached.

E. Switching and Settling Time

1. Switching Time

Switching time is defined as the time from when the control voltage crosses 50% of its final value to when the RF output reaches 10% or 90% of its target voltage level (rising/falling edge respectively). This is demonstrated in **Figure 16**. Switching time is a function of the gate's R-C time constant, so it is a controllable parameter for designers. However, in typical SOI switches, there are tradeoffs for reducing the R-C time constant.* Reducing the resistance improves switching time but increases the low-side frequency corner, forcing designers to choose between low frequency handling and fast switching time. Alternatively, reducing capacitance to improve switching time directly impacts the switch's loss since C is a function of FET size. Because of these tradeoffs, some switches are intentionally designed to have slower switching times to increase the power handling, reduce loss, or decrease the low frequency operation threshold. In contrast to typical switch tradeoffs, Marki Microwave offers FastSwitch™ technology that maintains fast switching time, low frequency operation, and high-power handling, which will be discussed in Section V.

** This excludes Marki Microwave's proprietary FastSwitch™ SOI CMOS technology. Discussion of FastSwitch™ technology will be addressed in Section **.*

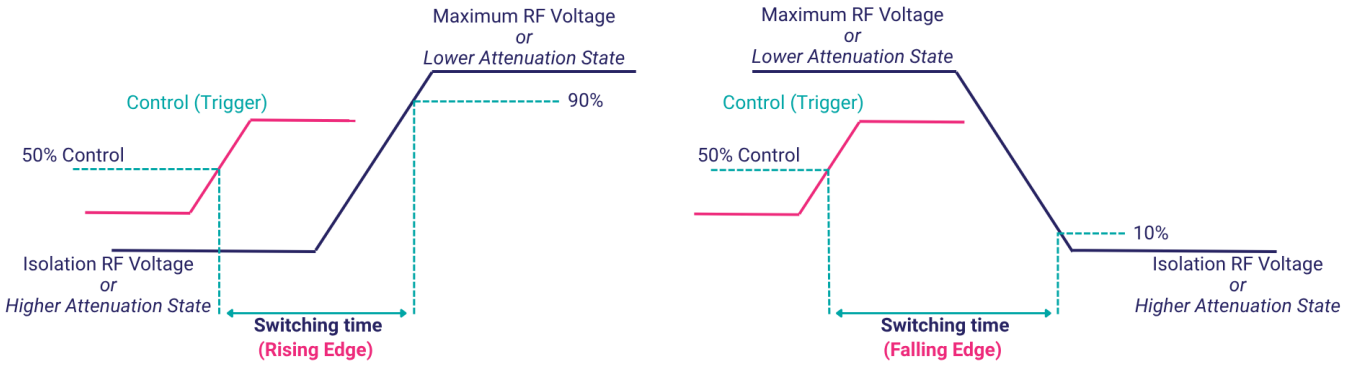


***Fig. 16**: Visual representation of switching time.*

2. Settling Time

Settling time is a function of switching time and gate lag; it is defined as the time from the 50% voltage control crossing until the RF output is within 0.1 dB of its steady state power (**Figure 17**). By definition, it cannot be lower than the designed switching time. The gate lag is defined by the underlying technology, which contributes to Marki's choice of SOI technology. SOI has an inherently low gate lag, unlike other comparable technologies. GaAs, for example, has a slow settling time even if the switching time is fast. III-V semiconductors generally have slower settling times due to defects and surface states. The electric field created when a reverse gate bias is applied to the transistor causes the electrons to tunnel away from the gate electrode and into the defect and surface state traps. This is one contributor to why test and measurement groups have historically gravitated to SOI switches, and why that trend is expected to continue.

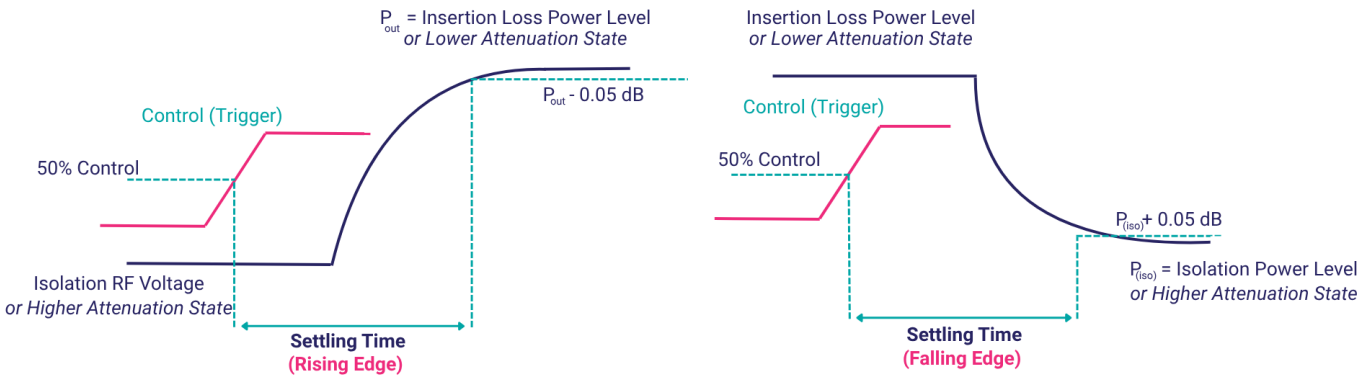


***Fig. 17**: Visual representation of settling time.*

3. Switching Rate

Switching time and settling time both contribute to the switching rate — the rate at which the switch can consecutively change states without RF performance degradation. The switching rate is also governed by the voltage and power regulation circuits that are used to bias the switch, depending on the technology, and whether such circuits are included in the switch die or placed elsewhere in the system. The switching rate is visually represented in **Figure 18** and mathematically defined in **Equation 2**.

$$Switching\ Rate = \frac{2}{T_{ctrl}} \tag{2}$$

V1	RFC-RF1	RFC-RF2
0	OFF	ON
1	ON	OFF

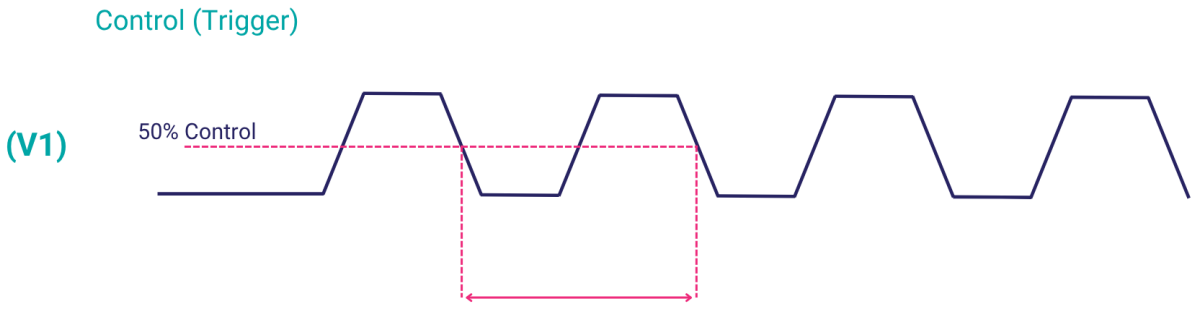


***Fig. 18**: Visual representation of the switching rate.*

4. Spurs

While spurs are usually associated with mixers, they can also appear in switches due to the charge pumps needed to produce the negative bias voltage to turn OFF FETs. For switches that contain their own supply management, spurs share characteristics:

- Fundamental spur frequency is typically 6 to 10 MHz, with lower-power harmonics.
- Spur level is typically below −100 dBm and varies by device and layout.
- Spur power is spread across approximately 10 to 100 kHz of bandwidth.
- Measured spur level depends strongly on spectrum analyzer resolution bandwidth (RBW). Unlike conventional spur measurements, reducing RBW will result in lower measured levels, since only a fraction of the spread power is captured in the narrower filter.

For switches with an external VSS pin, if an external negative supply is connected, the internal charge pump can be disabled to eliminate these spurs altogether. An external supply can be a useful solution for non-constrained systems given its spur elimination and positive impact on switching rate.

F. Additional Specifications

Different applications require different metrics- specifically, engineers design switches to accommodate system insertion loss, isolation, power handling, timing needs, and spurious performance needs. However, like all RF product families, there are a variety of other metrics that effect the overall system performance. SOI technology continues to perform well in these lesser-known categories.

For example, SOI is more immune to latch-up. “Latch-up” is the triggering of an internal parasitic feedback circuit that disrupts proper functioning. It can be caused by a single event upset, such as heavy ions or protons from cosmic rays or solar flares. As consumers strive to reduce risk and commercial space customers implement COTS products in their systems, the importance of latch-up risk reduction is growing. Latch-up can only be terminated in two ways, either by power cycling the part or destroying the part. Since SOI is very low loss, they are less susceptible to latch-up. This improves a failure mode and is a key indicator of the technology’s performance stability and reliability.

In addition to lower latch-up susceptibility, SOI CMOS switches do not require blocking caps if there is no external DC present. Within the IC, there is no DC generated on the RF lines, allowing parts to be cascaded without losing bandwidth from blocking capacitor filtering. With this, performance does not need to be “tuned” for narrowband performance, but rather has reliable performance across a broad bandwidth.

IV. HOT-SWITCHING

Hot-switching of an SPnT is when power input into the common port is continuously present while the part is switching. Hot switching can benefit time, simplicity, and system continuity; however, it introduces risk since there is a momentary discontinuity for the flowing signal. Some technologies, such as MEMS, have zero or limited tolerance to hot-switching and can suffer permanent failure from it. In contrast, SOI is tolerant to hot-switching if designed and operated properly.

While mechanical switches are at risk of melting, fusing, or cratering, SOI switches are vulnerable due to the voltage and current transients during the hot switching event. To better understand the robustness of Marki Microwave switches, Marki engineers hot-switched several parts at their maximum rated CW power for at least one million cycles each.

During this test, Marki engineers looked for two types of failures: hard failures and soft failures. Hard failures were defined as a drastic change in performance or complete shut-down of the part or its functionality. Soft failures were defined as a small variation in performance, similar to "wear and tear" indicators. In all the parts selected and tested, 100% passed without hard or soft failures. This means that after 1 million hot-switching cycles at maximum rated CW power, all the parts had insignificant variations in performance. In conclusion, Marki SOI switches are eligible for hot-switching and can withstand a large number of events.*

** For hot-switching intensive applications, customers are encouraged to perform their own robustness testing.*

V. FASTSWITCH™ TECHNOLOGY

For all solid state switch technologies, switching speed has always been a trade-off with maximum and minimum frequency, loss, and maximum power. With Marki Microwave's FastSwitch™ SOI technology, this is no longer the case. FastSwitch™ implements a novel on-chip driver that uses an increased supply voltage to speed up SOI switches, allowing other tradeoffs to relax. FastSwitch™ reduces the switching speed by 5, 10, or even 100x, reaching GaN switching speeds while maintaining the loss, bandwidth, scalability, and cost benefits of SOI technology. Unlike GaN, FastSwitch technology uses a larger positive supply rather than a larger negative supply for operation. This simplifies the system design, as there are often large positive supplies available for power amplifier operation. The power handling benefits of FastSwitch™ versus other SOI technologies are shown in **Figure 19**. FastSwitch™ is a proprietary technology, so it is best represented by its applications since its technical foundation cannot be discussed.

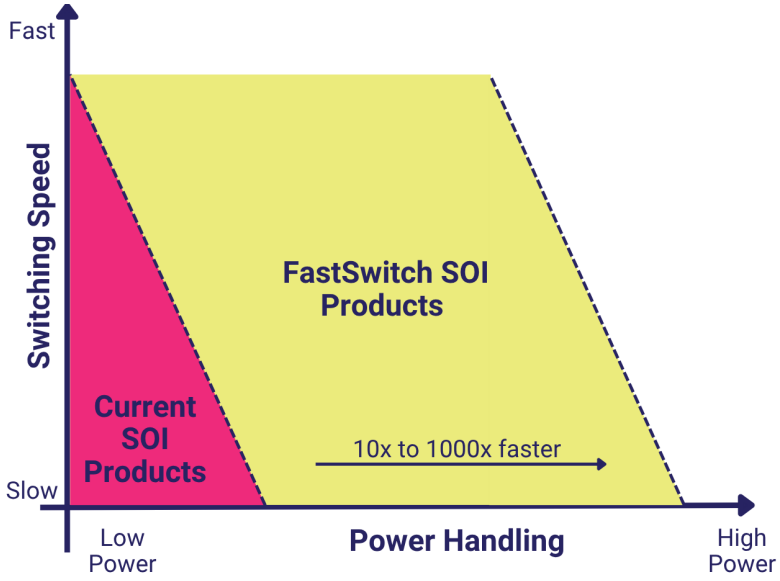


***Fig. 19**: Demonstrated improved power handling of FastSwitch™ technology.*

VI. SWITCH APPLICATIONS

RF switches have an endless list of applications given their ubiquitous presence in RF systems. They have notable consequences in three critical domains: pulsed radar systems, electronic warfare platforms, and 5G/6G wireless systems.

Radar systems rely on transmit/receive (T/R) switches to toggle the antenna alternately to the transmitter and receiver. During the transmit phase, the switch must pass a high-power pulse with minimal loss, while during the receive phase, it must protect the sensitive receiver front-end and recover quickly. Slow recovery leads to larger "blind spots" for the radar, which is a key metric for measuring radar performance. Other metrics include power handling, which determines the maximum detection range, insertion loss, which impacts transmitted power and received signal sensitivity, and switching time, which determines the minimum detectable range in addition to blind spot size and placement. Any degradation in these metrics, in the switch or other components, negatively effects warning time, tracking accuracy, and system utility.

In existing switch technologies, the fundamental tradeoffs, as discussed in Section III, can force system designers to accept compromises that reduce effective range by up to 50%. Tradeoffs such as high-power handling necessitating larger switches or low frequencies demanding slower switching rates are unacceptable as incoming signals increase in volume and weapons increase in stealth. Before FastSwitch™, no single switch topology could achieve top performance in each of these parameters, increasing danger to systems reliant on radars.

Similar to radar, airborne electronic warfare (EW) systems rely on T/R switches. EW systems use T/R switches as part of a rapid sense-identify-respond loop: a nosecone phased array receives an adversary's radar emission, a digital processor identifies the signature and threat, and the EW system transmits a high-power jamming or spoofing signal. The catch for EW systems is that this loop must complete in between the adversary's radar pulses, demanding an extremely fast process. If the jamming signal is not strong enough, it will not effectively mask or spoof the aircraft's radar return. On the other hand, if the loop is not finished within the next pulse, the spoofing signal will not be transmitted in time. Prior to FastSwitch™, this was a key technology gap, placing constraints on the effectiveness of airborne EW systems. As shown in Figure 19, FastSwitch™ fills this gap by providing fast switching at high powers.

The final critical domain that will rely on fast, high-power switching is 5G/6G networking. They key parameter for success of cellular communication systems is latency. Latency is the total turnaround time for a communication link. Historically, latency has been a benefit rather than a necessity; however, as industrialists continue to release autonomous vehicles, industrial automation, and AI-driven real time decision systems, latency will become a key success and safety parameter. Further, the switching time of RF switches in base station and user equipment phased arrays cannot exceed 0.1% of the total latency requirement. **Table 4** shows the historic and expected latency and switching time requirements for the different wireless cellular generations.

Generation	Latency Requirement	Switching Time
2G	<1 s	1 ms
3G	<500 ms	500 µs
4G	<100 ms	100 µs
5G	<1 ms	1 µs
6G	<10 µs	10ns

***Table 4**: Historic and expected latency and switching time requirements for cellular generations.*

The transition from 5G to 6G is a challenging inflection point. In addition to the increase in speed, the increase in data density demands higher power handling. This dual requirement brings engineers, once again, to the standard switch tradeoff: high-power versus fast switching, creating another demand for Marki Microwave's FastSwitch™ technology.

VII. CONCLUSION

Switching is a ubiquitous technology, but its pervasive nature in RF is not due to the ease of technology development, but to the necessity of it. RF switching can be accomplished through electromechanical switching or solid-state switching, including MEMS, PIN diodes, GaAs substrates, and SOI CMOS, with one technology standing out above the rest: SOI.

SOI switching shows benefits in insertion loss, $R_{ON}*_{COFF}$, isolation, power handling, linearity, and timing. It also has great benefits in spurious performance and supports hot switching, giving users flexibility as systems evolve. With FastSwitch™ technology, SOI CMOS fills a historic gap in switch performance: combining high-power and high-speed switching while maintaining loss, isolation, linearity, and SWaP. This eliminates the speed/power compromise engineers have historically had to make in radar, electronic warfare, and wireless communication systems, creating a safer physical and technological environment.