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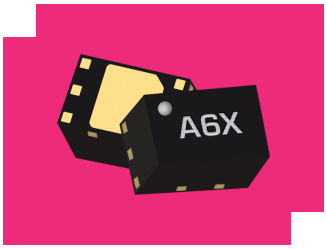
ADM-8096PSM

0.09 - 6 GHz High Dynamic Range Gain Block

DEVICE OVERVIEW

General Description

The ADM-8096PSM is a high-linearity low noise amplifier capable of providing +23 dBm output power up to 6 GHz. The ADM-8096PSM can serve either as a linear signal amplifier, or as a saturated driver amplifier for H- or S-diode mixers. The amplifier has excellent return losses and gain flatness.



Download s-parameters here

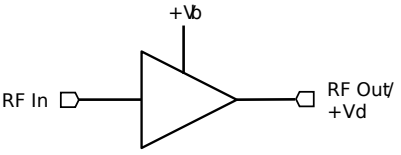
Features

- +23 dBm output power
- +22 dB gain
- 5 dB noise figure
- Excellent Gain flatness
- No negative bias required

Applications

- Mobile test and measurement equipment
- Radar and satellite communications
- 5G transceivers
- Driver Amplifier for H and S - Diode Mixers

Functional Block Diagram



Part Ordering Options

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
ADM-8096PSM	0.09 - 6 GHz High Dynamic Range Gain Block	DFN	REACH RoHS	Released	EAR99
EVB-ADM-8096P	Evaluation Board, 0.09 - 6 GHz High Dynamic Range Gain Block	EVB	REACH RoHS	Released	EAR99

Table Of Contents

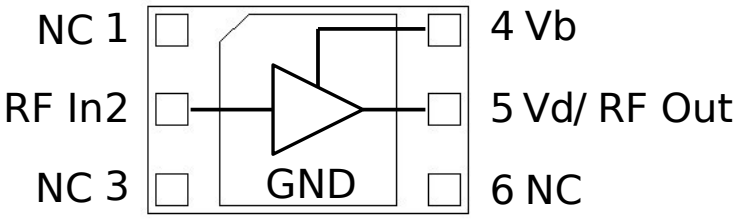
Revision History

Revision Code	Revision Date	Comment
-	2022-09-01	Initial Release
A	2022-10-01	Package Drawing Updated
B	2026-02-26	ESD Class Added

Port Configuration and Functions

Port Diagram

A port diagram of the ADM-8096PSM DFN package is shown below (X-ray view from the top). The pin functions are detailed below.



Port Functions

Port	Function	Description	DC Equivalent Circuit
1,3,6	Gnd	These pins should be connected to ground.	-
2	RF Input	Pin 2 is the RF Input port of the amplifier. It is internally RF matched to 50 Ω and requires an external DC blocking cap.	-
4	Vb	Pin 4 provides DC bias to the amplifier. Placement of an external series bias resistor allows this pin to be supplied by the same supply line providing 5V to Pin 5. For normal operation, this pin can be left floating. DO NOT GROUND this pin. Device drain current will change proportional to the current flowing into this pin. RF performance can be balanced with DC power consumption by adjusting the current into this pin.	-
5	RF Out / Vd	Pin 5 is the RF Output port and is also the Vd port providing the main power supply to the amplifier. This pin is DC coupled and requires an external bias-T or discrete choke and DC blocking capacitor. This port is RF matched to 50 Ω. DC voltage at this pin should be set to 5V for normal operation.	-
Paddle	Gnd	Package ground paddle must be connected to a DC/RF ground potential with high thermal and electrical conductivity.	-

Specifications

Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If any one of these limits are exceeded, the device may become inoperable or have a reduced lifetime. Reliability limits are individual, instantaneous catastrophic limits only. Functional operation limits are indicated below. Operation of the device at multiple absolute maximum limits or for extended periods at a single limit can cause degradation and damage to the device.

Parameter	Maximum Rating	Unit
Bias Voltage (Vb)	8	V
Drain Current (No RF Applied)	222	mA
Drain Supply Voltage (Vd)	8	V
Maximum Operating Temperature for MTTF > 1E6 hours	85	°C
Maximum Storage Temperature	125	°C
Max Junction Temperature for MTTF of 1E6 hours	175	°C
Max Power Dissipation for MTTF of 1E6 hours	0.72	W
Minimum Operating Temperature for MTTF > 1E6 hours	-40	°C
Minimum Storage Temperature	-65	°C
RF Input Power	15	dBm
θ_Jc, Junction to Case Thermal Resistance	65	°C/W

Package Information

Parameter	Details	Rating
ESD	250 to < 500 Volts	HBM Class 1A
Weight	Package name: DFN	0.007g
Dimensions	-	1.3 x 2 mm
Moisture Sensitivity Level	-	MSL 1

Recommended Operating Conditions

The Recommended Operating Conditions indicate the limits, inside which the device should be operated, to guarantee the performance given in Electrical Specifications Operating outside these limits may not necessarily cause damage to the device, but the performance may degrade outside the limits of the electrical specifications. For limits, above which damage may occur, see Absolute Maximum Ratings.

Parameter	Min	Nominal	Max	Unit
Ambient Temperature	-40	25	85	°C
Power Supply DC Voltage (Vd)	3	5	6	V
Power Supply DC Current (Id) (No RF Input) [1]	31	58	71	mA
Input Power for Saturation	2	4	6	dBm

[1] Recommended operating current conditions without RF input applied.

Sequencing Requirements

There is no sequencing required to power up or power down the amplifier. The amplifier must have an output load connected during operation.

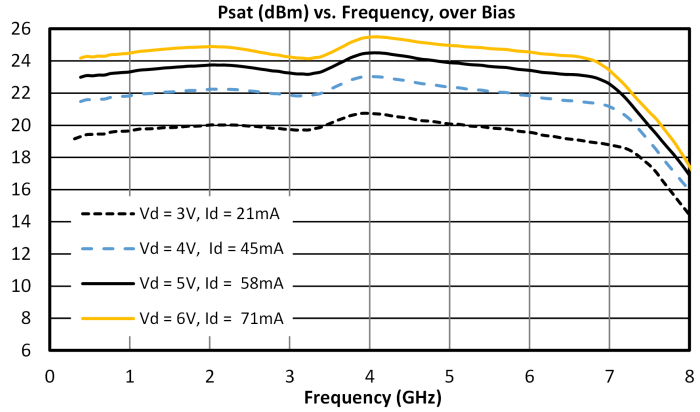
Electrical Specifications

Unless otherwise specified, electrical specifications apply at TA=+25°C, Vd = 5 V, Vb = Float.

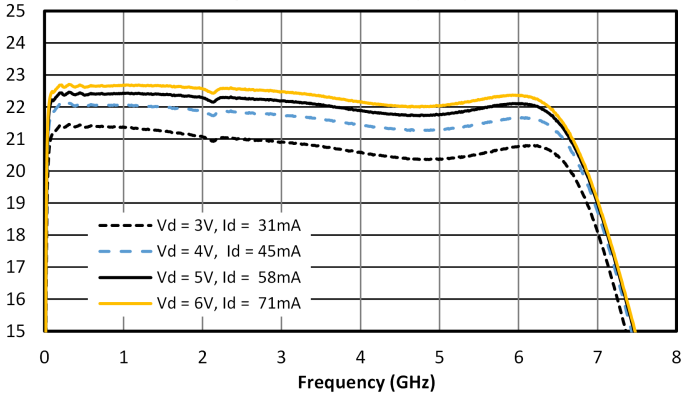
Parameter	Test Conditions	Minimum Frequency (GHz)	Maximum Frequency (GHz)	Min	Typ	Max	Unit
Current Consumption	Vd = 5 V, no RF input	-	-	-	58	-	mA
Input IP3	Vd = 5 V, Pin = -15 dBm per tone, 10 MHz tone spacing	0.09	6	-	11	-	dBm
Input Power for Saturation	Vd = 5V	0.09	6	-	4	-	dBm
Input Return Loss	Vd = 5 V, Pin = -20 dBm	0.09	6	-	15	-	dB
Noise Figure	Vd = 5 V, Pin = -20 dBm	0.09	3	-	1.5	-	dB
Noise Figure	Vd = 5 V, Pin = -20 dBm	3	6	-	1.9	-	dB
Output IP2	Vd = 5 V, Pin = -15 dBm per tone, 10 MHz tone spacing	0.09	6	-	35	-	dBm
Output IP3	Vd = 5 V, Pin = -15 dBm per tone, 10 MHz tone spacing	0.09	6	-	33	-	dBm
Output P1dB	Vd = 5V	0.09	6	-	21	-	dBm
Output Return Loss	Vd = 5 V, Pin = -20 dBm	0.09	6	-	17	-	dB
Reverse Isolation	Vd = 5 V, Pin = -20 dBm	0.09	6	-	28	-	dB
Saturated Output Power	Vd = 5 V	0.09	6	-	23	-	dBm
Small Signal Gain	Vd = 5 V, Pin = -20 dBm	0.09	6	-	22	-	dB

Typical Performance Plots

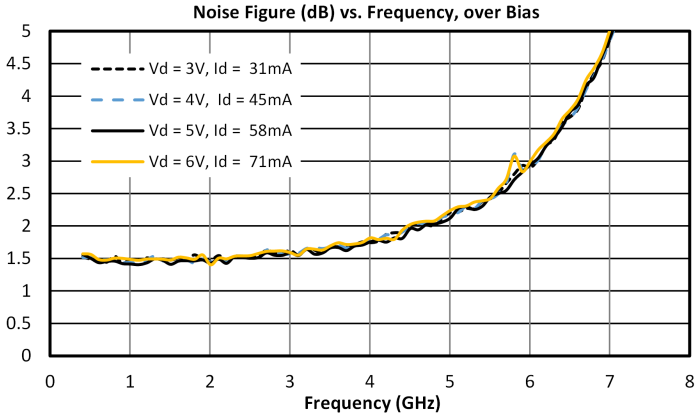
Psat (dBm) vs. Frequency, over Bias



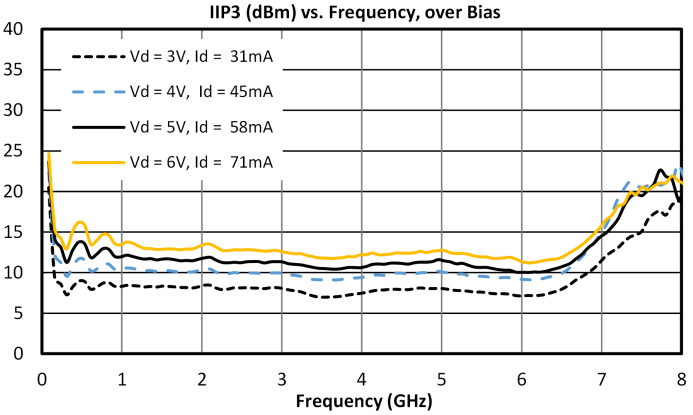
Small Signal Gain (dB) vs. Frequency, over Bias



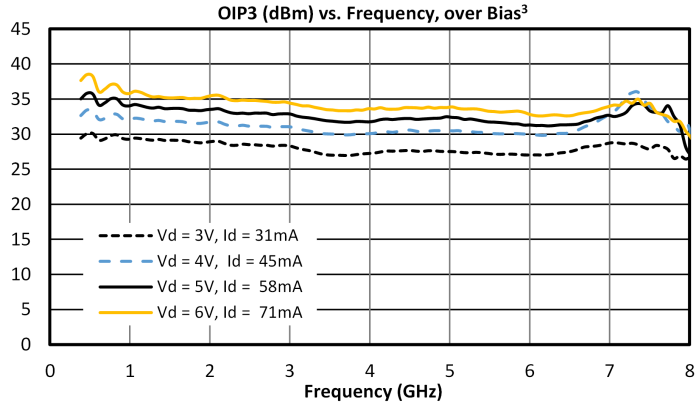
Noise Figure (dB) vs. Frequency, over Bias



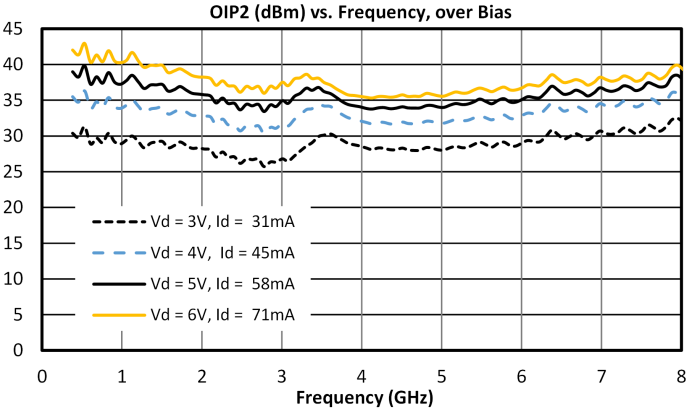
IIP3 (dBm) vs. Frequency, over Bias



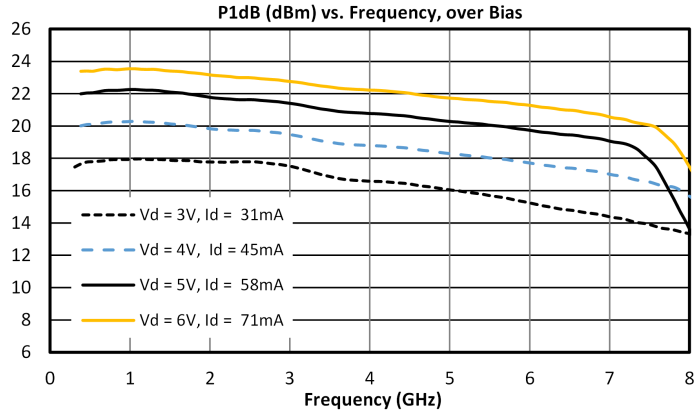
OIP3 (dBm) vs. Frequency, over Bias[3]



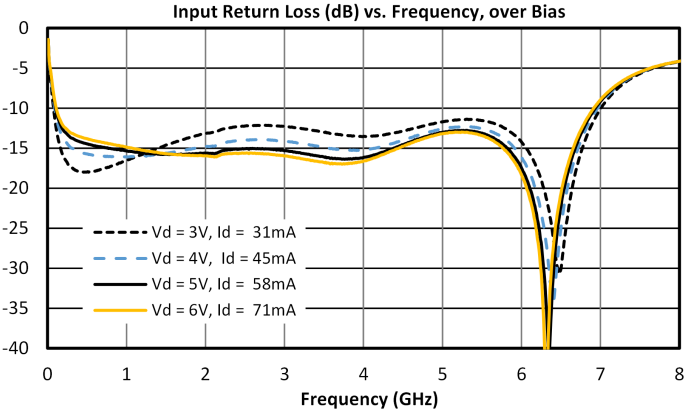
OIP2 (dBm) vs. Frequency, over Bias



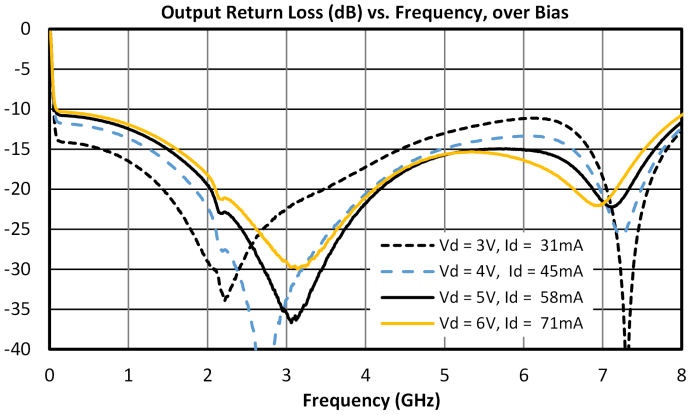
P1dB (dBm) vs. Frequency, over Bias



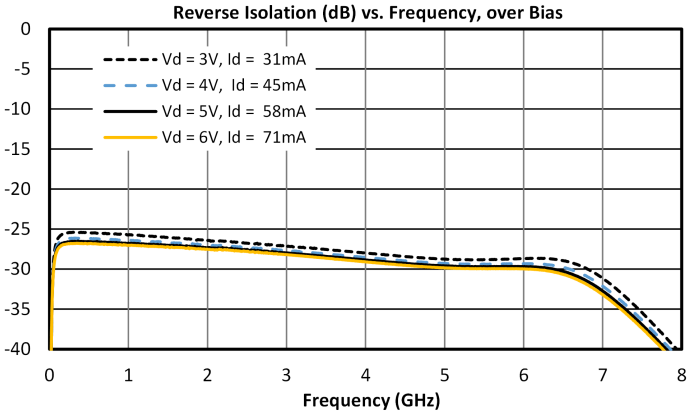
Input Return Loss (dB) vs. Frequency, over Bias



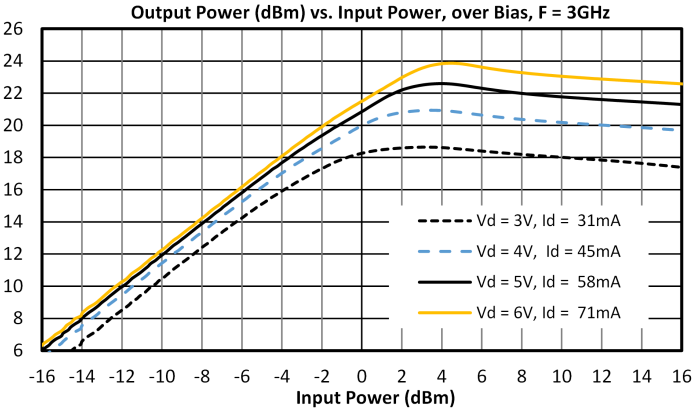
Output Return Loss (dB) vs. Frequency, over Bias



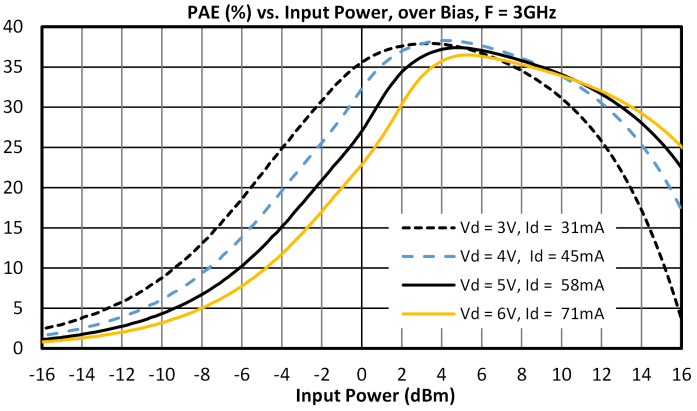
Reverse Isolation (dB) vs. Frequency, over Bias



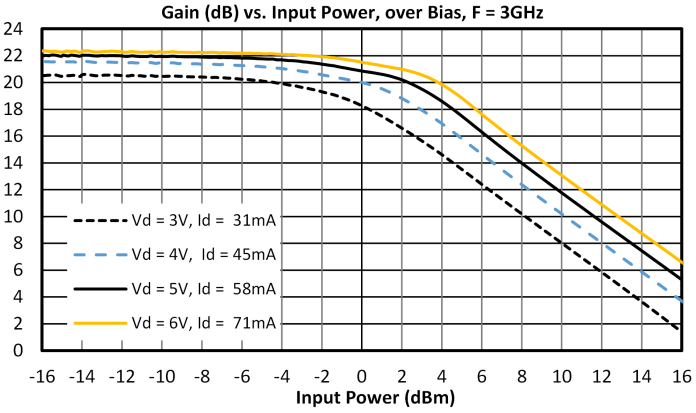
Output Power (dBm) vs. Input Power, over Bias, F = 3GHz



PAE (%) vs. Input Power, over Bias, F = 3GHz



Gain (dB) vs. Input Power, over Bias, F = 3GHz

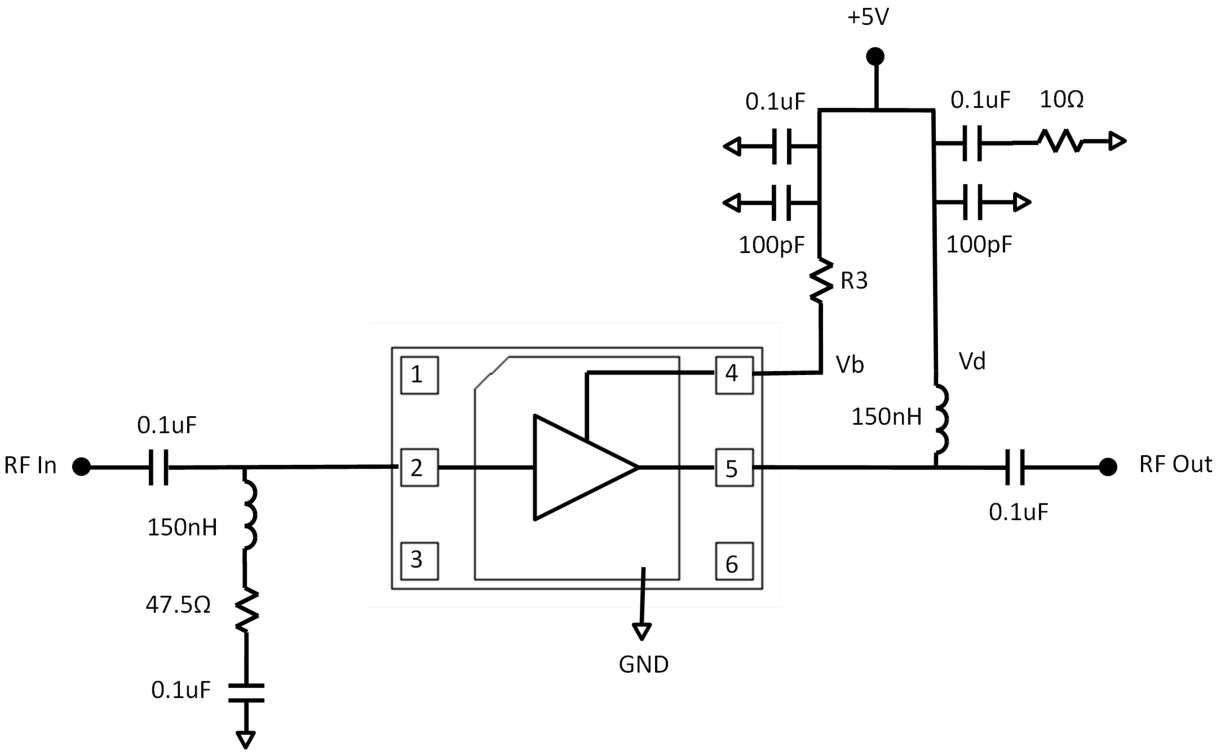


Application Information

Application Circuit

Below is the recommended application circuit for the ADM-8096PSM. DC power is supplied to RF Out/Vd pin 5 via a 150 nH choke inductor. Supply bypassing is provided by 100pf and 0.1uF capacitors. Drain current Id can be controlled by applying voltage to Vb pin 4. Drain current Id is adjusted proportionally to the current flowing into pin 4 with higher Vb and Ib resulting in increased current Id. Amplifier performance can therefore be optimized for specific applications by adjusting the value of series resistor R3 on the Vb line. In particular, OIP3 across the band and especially at low frequencies can be improved from that shown in section 3.6 by increasing current into pin 4. The OIP3 can be improved by up to 5dB with the tradeoff being increased quiescent DC power consumption. EVB-ADM-8096P has provisions for an 0201 SMD resistor to be placed in series on the Vb line; However, the default configuration is to leave this resistor un-populated and leave the Vb pin un-connected or floating. The ADM-8096PSM requires an RF input matching network at RF In pin 2 as shown. DC blocking capacitors are also required at RF input and output pins as shown. Note that EVB-ADM-8096P does not include DC blocking capacitors and must be externally blocked. See section 5.4 for more details on the EVB circuit layout and component values. Contact support@markimicrowave.com if you would like help creating an alternative application circuit for your system's requirements.

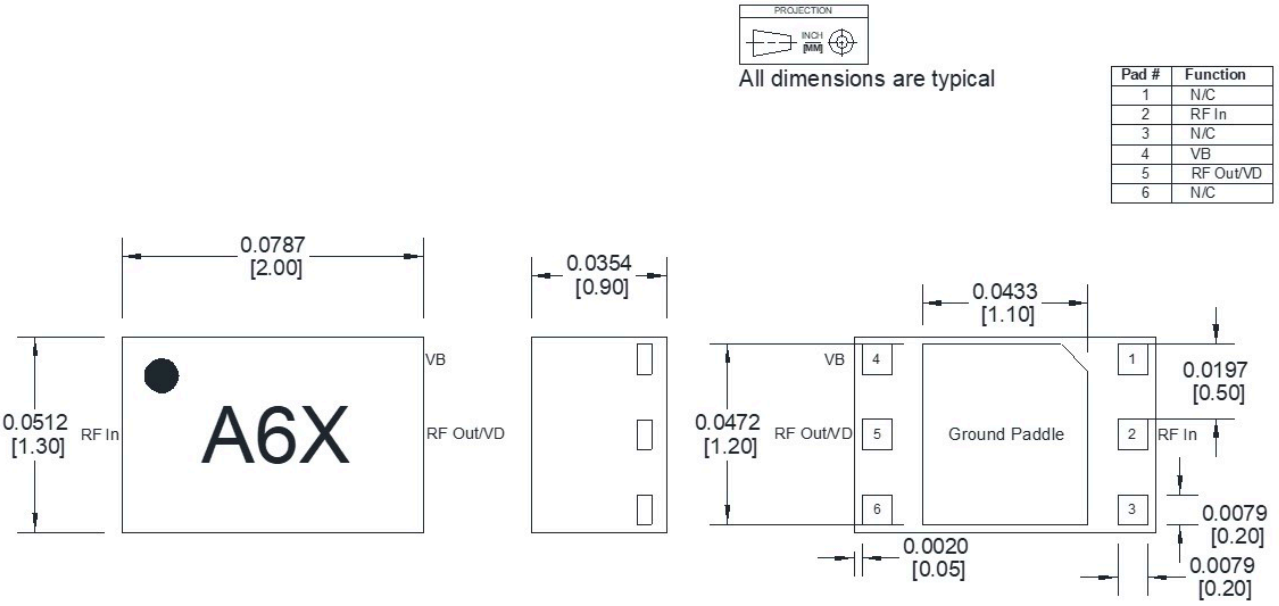
Application Circuit



Mechanical Data

Outline Drawing

Download : Outline 2D Drawing | Outline 3D Drawing | Outline 3D STP

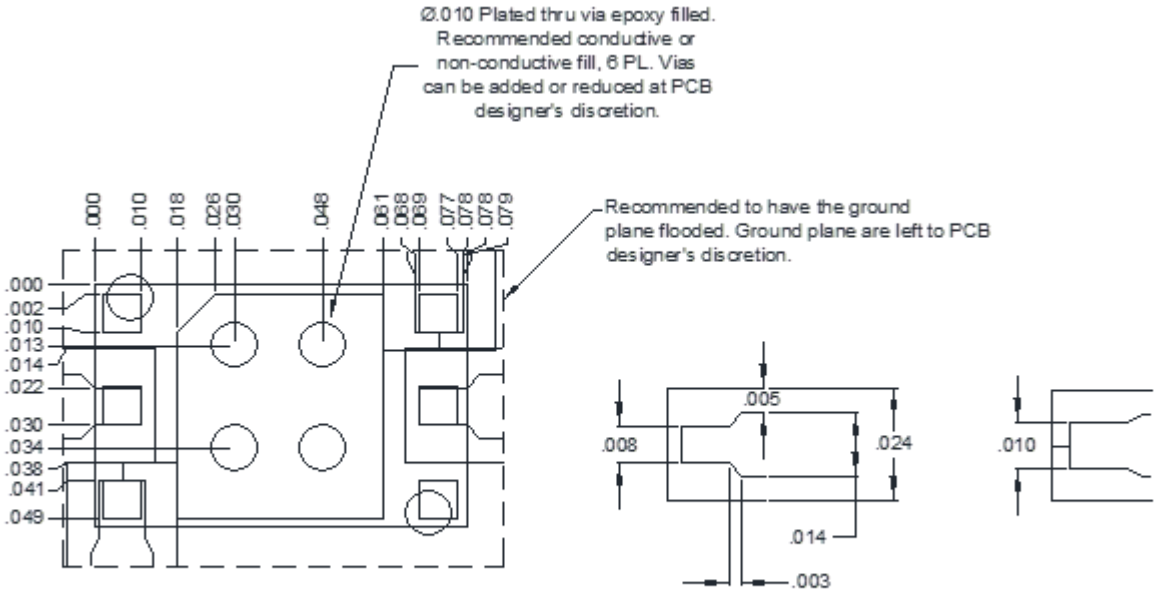


Pad #	Function
1	N/C
2	RF In
3	N/C
4	VB
5	RF Out/VD
6	N/C

1) Substrate material is LCP
2) I/O Leads and Die Paddle is (from base to finish):
   a. Ni: 0.5 um MIN
   b. Pd: 0.02 um MIN
   c. Au: 0.05 um MAX
3) All unconnected pins should be attached to PCB RF ground.

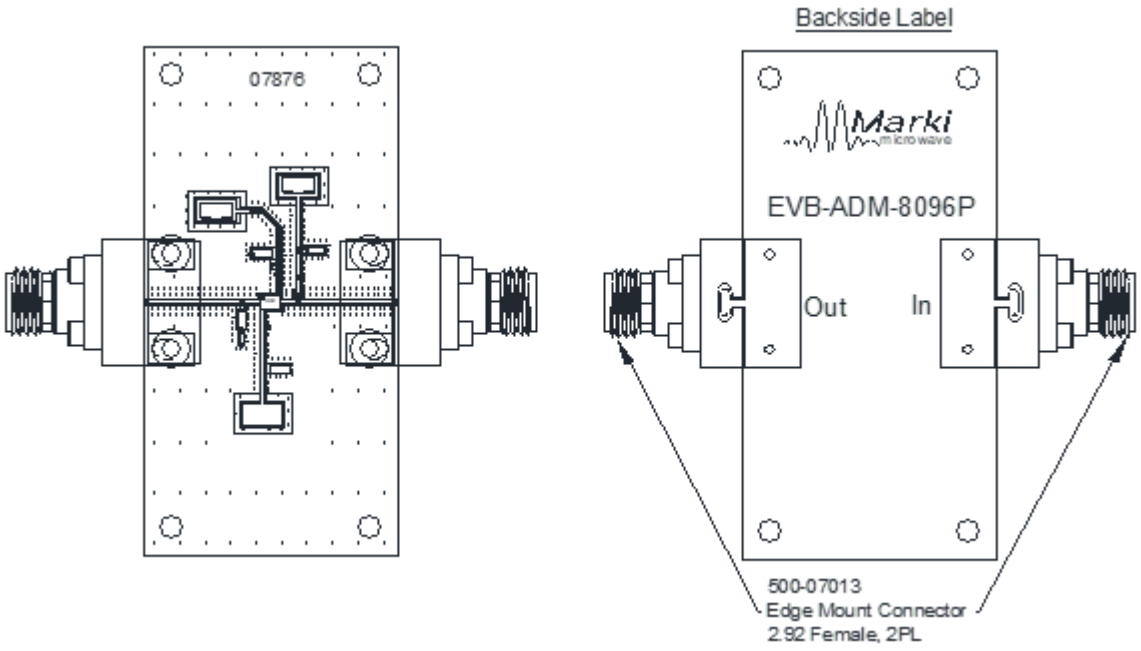
Footprint Image

Download : Footprint Drawing



The landing pattern is to be used on Rogers 4003, 0.008" thick, $\frac{1}{2}$ Oz Cu.

Evaluation Board - Outline Drawing



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