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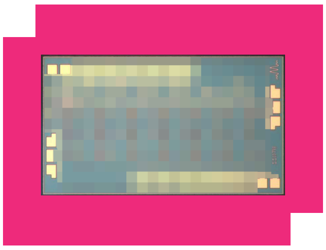
AMM-11561CH

0.01 – 30 GHz High Frequency Distributed Driver Amplifier

DEVICE OVERVIEW

General Description

The AMM-11561CH is a wideband GaAs distributed amplifier covering 0.01 to 30 GHz, delivering 15.7 dB of small-signal gain, high output power, and linearity. It provides up to +27 dBm saturated output power, with output IP3 up to +33 dBm. Operating from a +12V supply at 220 mA typical current, the amplifier is internally matched to 50 Ω at both the RF input and output ports. These features make it well-suited for wideband driver stages in RF/mmWave front ends, test and measurement instrumentation, electronic warfare, and general-purpose broadband gain block applications.



Download s-parameters here

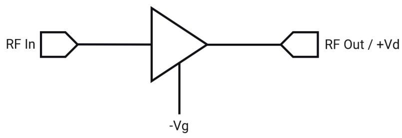
Features

- High Frequency Wideband Operation, 0.01 to 30 GHz
- High Saturated Output Power, +27 dBm Typical
- Minimal Application Circuit

Applications

- SATCOM
- 5G Transceivers
- Test and Measurement Equipment

Functional Block Diagram



Part Ordering Options

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
AMM-11561CH	0.01 – 30 GHz High Frequency Distributed Driver Amplifier	CH	REACH RoHS	Released	EAR99

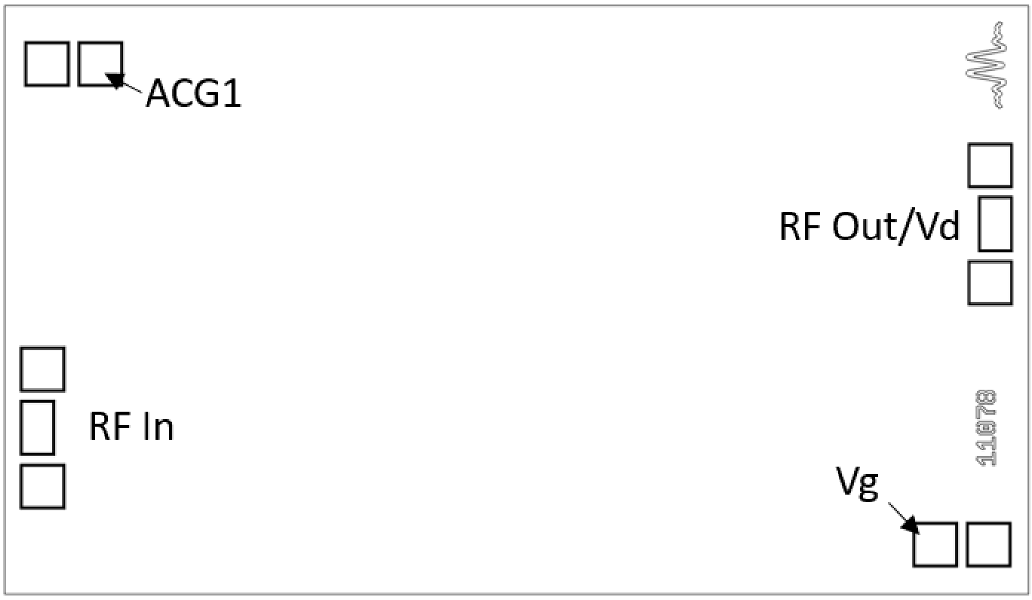
Table Of Contents

Revision History

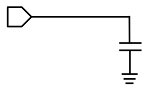
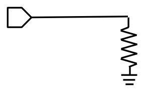
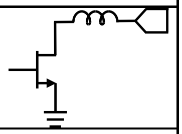
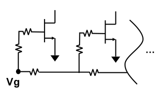
Revision Code	Revision Date	Comment
-	2026-06-04	Initial Release

Port Configuration and Functions

Port Diagram



Port Functions

Port	Function	Description	DC Equivalent Circuit
ACG1	External Chip Capacitor	The ACG1 pad provides additional off chip bypass capacitance. A 0.1uF chip capacitor is recommended.	
GND	Ground	Bottom side must be connected to a DC/RF ground potential with high thermal and electrical conductivity.	
RF In	RF Input	This is the RF Input port of the amplifier die. It is RF matched to 50 Ω and requires a DC blocking capacitor.	
RF Out	RF Output	The RF Out/ Vd pad supplies DC voltage to the drain of the amplifier and also acts as the RF output. This pad requires an external bias-tee.	
Vg	Gate Bias Voltage Pad	The Vg pad is connected resistively on chip. The user should apply between -0.15V and -0.35V to Vg pad before applying positive DC voltage to any Vd port. Lower (more negative) voltages on a Vg pad will result in lower drain current and lower small signal gain.	

Specifications

Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If these limits are exceeded, the device may become inoperable or have a reduced lifetime. This amplifier is designed and characterized in a 50Ω system, and operation in a reflective environment can cause performance degradation.

Parameter	Maximum Rating	Unit
Continuous Power Dissipation (PDISS) (at 85 ˚C case temp.)	3	W
Maximum Operating Temperature [1]	85	˚C
Maximum Storage Temperature	150	˚C
Max Junction Temperature for MTTF > 1E6 Hours	175	˚C
Minimum Operating Temperature	-40	˚C
Minimum Storage Temperature	-65	˚C
Negative Bias Voltage (Vg)	-2	V
Positive Drain Supply Current (Id) (with RF Input)	250	mA
Positive Drain Supply Voltage (Vd)	12	V
RF Input Power	20	dBm
Thermal Resistance, θJC	15	ºC/W

[1] Low thermal resistance die attach to thermal ground is necessary for MTTF > 1x10^6 hours

Package Information

Parameter	Details	Rating
ESD	< 250 Volts	HBM Class 0
Dimensions	-	1.38mm x 2.40mm

Recommended Operating Conditions

The Recommended Operating Conditions indicate the limits, inside which the device should be operated, to guarantee the performance given in Electrical Specifications. Operating outside these limits may not necessarily cause damage to the device, but the performance may degrade outside the limits of the electrical specifications. For limits, above which damage may occur, see Absolute Maximum Ratings. Power Supply DC current should be modified by changing bias voltage Vg to maintain junction temperature within MTTF target for given operating conditions.

Parameter	Min	Nominal	Max	Unit
Power Supply DC Voltage (Vd)	10	12	12	V
Power Supply DC Current (Id) (No RF Input)	150	220	230	mA
Ambient Temperature	-40	25	85	˚C
Negative Bias Voltage (Vg)	-0.35	-0.25	-0.15	V
Input Power for Saturation	10	11	15	dBm

Sequencing Requirements

Turn-on Procedure:
1. Apply negative bias to Vg
2. Apply Vd

Turn-off Procedure:
1. Turn off Vd
2. Turn off Vg

Note: RF input power can be injected at any moment in the bias sequencing procedure.

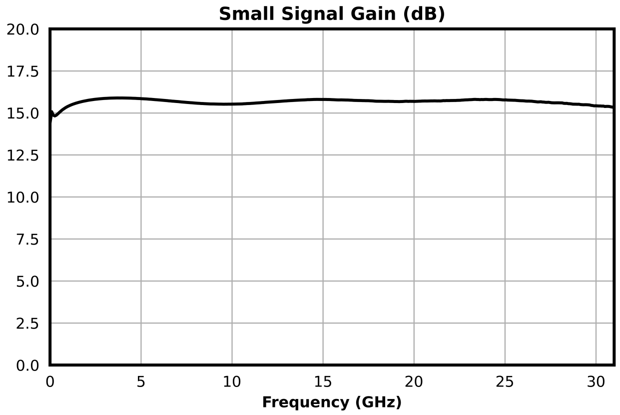
Electrical Specifications

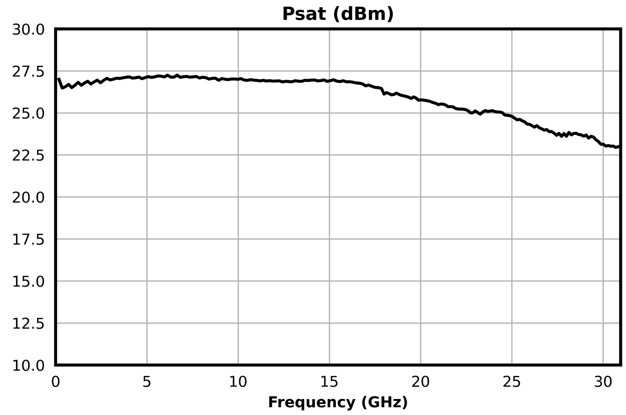
The electrical specifications apply at TA=+25°C in a 50Ω system. Min and Max limits apply only to our connectorized units and are guaranteed at TA=+25°C. Die are 100% DC tested and RF tested on a per lot basis

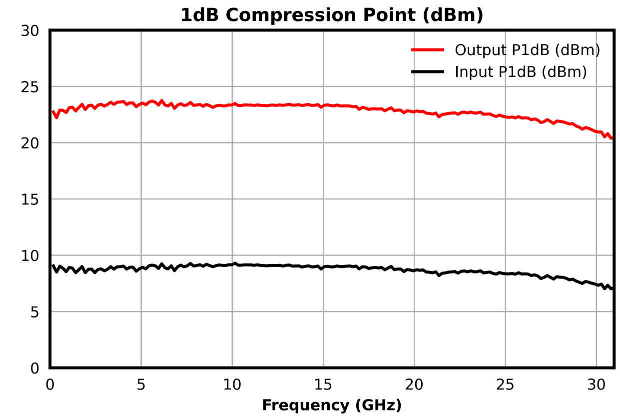
Parameter	Test Conditions	Minimum Frequency (GHz)	Maximum Frequency (GHz)	Min	Typ	Max	Unit
Small Signal Gain	Vd = +12V, Id = 220mA, Vg = -0.25V, Pin = -20dBm	0.01	30	-	15.7	-	dB
Input Return Loss	Vd = +12V, Id = 220mA, Vg = -0.25V, Pin = -20dBm	0.01	30	-	19	-	dB
Output Return Loss	Vd = +12V, Id = 220mA, Vg = -0.25V, Pin = -20dBm	0.01	30	-	20	-	dB
Reverse Isolation	Vd = +12V, Id = 220mA, Vg = -0.25V, Pin = -20dBm	0.01	30	-	54	-	dB
Psat	Vd = +12V, Id = 220mA, Vg = -0.25V,	0.01	30	-	27	-	dBm
Input P1dB	Vd = +12V, Id = 220mA, Vg = -0.25V	0.01	30	-	9	-	dBm
Output P1dB	Vd = +12V, Id = 220mA, Vg = -0.25V	0.01	30	-	23	-	dBm
Input IP3	Vd = +12V, Id = 220mA, Vg = -0.25V, Pin = -18dBm, 1MHz Spacing	0.01	30	-	18	-	dBm
Output IP3	Vd = +12V, Id = 220mA, Vg = -0.25V, Pin = -18dBm, 1MHz Spacing	0.01	30	-	33	-	dBm
Input IP2	Vd = +12V, Id = 220mA, Vg = -0.25V, Pin = -18dBm, 1MHz Spacing	0.01	30	-	23.5	-	dBm
Output IP2	Vd = +12V, Id = 220mA, Vg = -0.25V, Pin = -18dBm, 1MHz Spacing	0.01	30	-	38.5	-	dBm
Noise Figure	Vd = +12V, Id = 220mA, Vg = -0.25V	0.01	30	-	4.4	-	dB
Current Consumption	Vd= +12V, Vg = -0.25V	-	-	-	220	-	mA

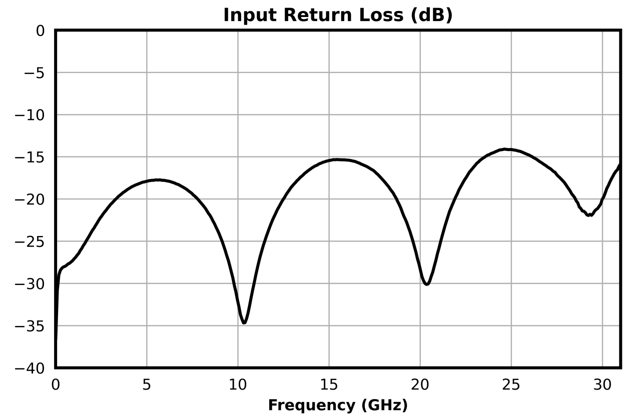
Low frequency performance dependent on application circuit. For operation under 10MHz see application circuit notes.

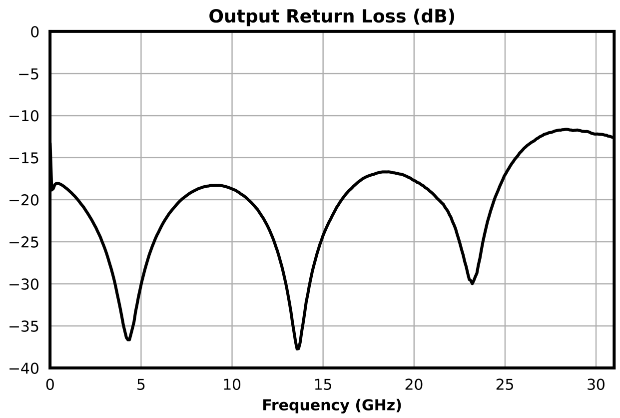
Typical Performance Plots

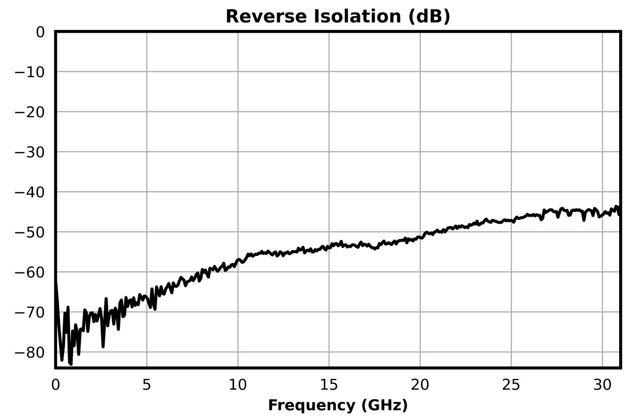


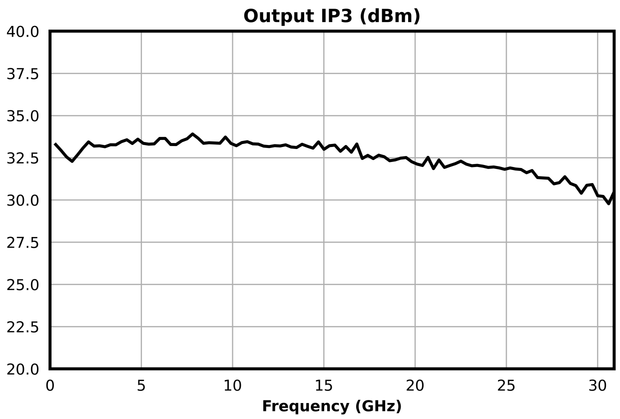


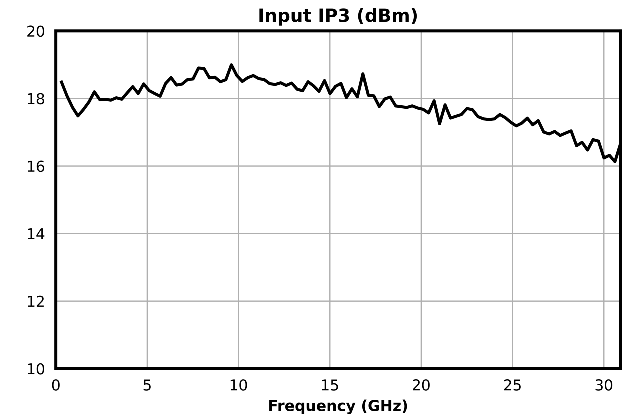


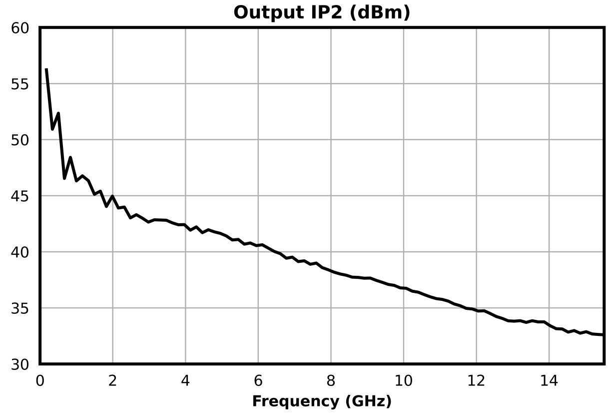


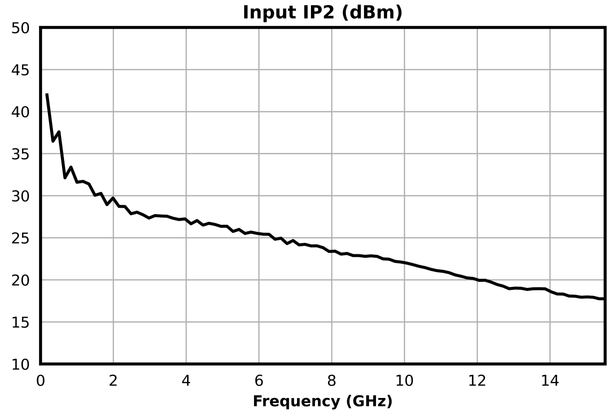


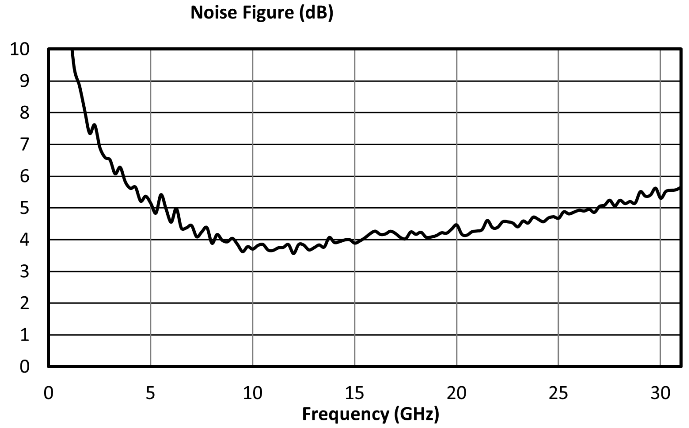







Output IP2 (dBm)
60
55
50
45
40
35
30
0
2
4
6
8
10
12
14
Frequency (GHz)

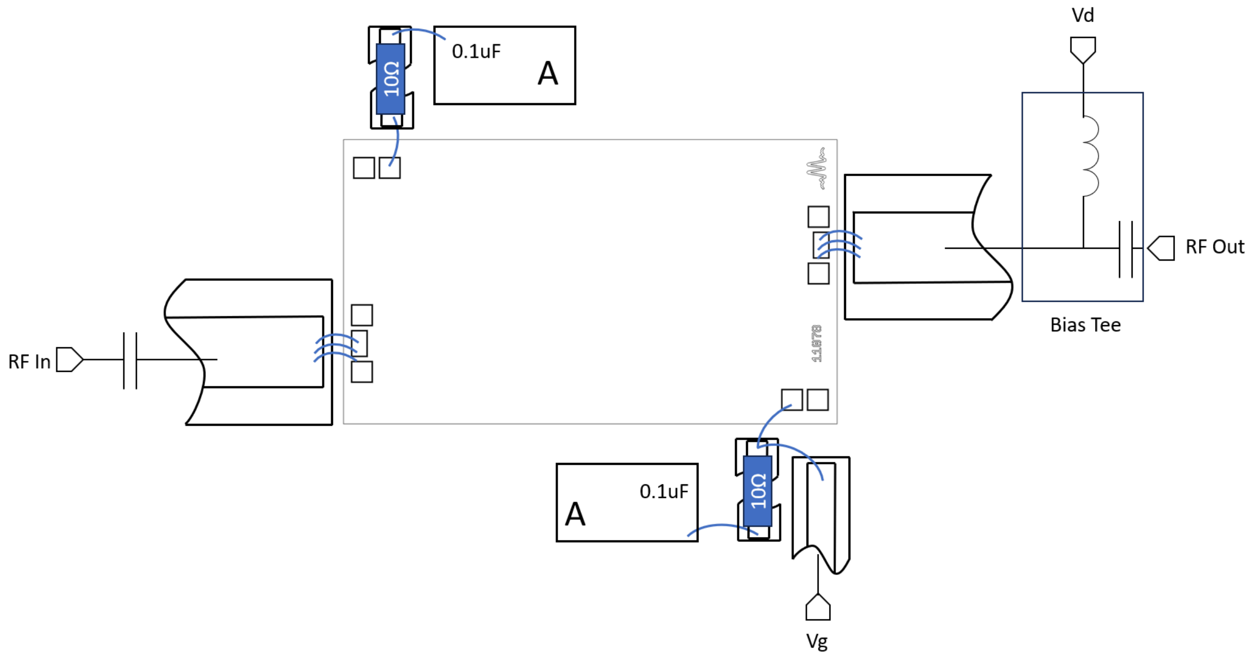

Input IP2 (dBm)
50
45
40
35
30
25
20
15
10
0
2
4
6
8
10
12
14
Frequency (GHz)


Noise Figure (dB)
10
9
8
7
6
5
4
3
2
1
0
0
5
10
15
20
25
30
Frequency (GHz)

Application Information

Below are the recommended application circuits for the AMM-11561CH. This application circuit is used for the performance plots shown in this datasheet. However, each PCB layout and environment is different which may require minor modifications of the biasing network.

Application Circuit



Application Circuit Description

Designator	Description	Sample Part Number
A	Presidio 0.1 µF + 1800 pF Capacitor	MVB4080X104ZGH5R3
B	PPI 10Ω Wire-bondable series resistor	PRT135-14x12x10A10R00FQE

Low Frequency Operation

The AMM-11561CH can be used at low frequency approaching DC. Operation below 10MHz requires using larger bypass capacitors to provide AC ground across the frequency range of interest. It is recommended to place additional bypass capacitance in parallel with designator **A**. For example, if operation is desired to 100KHz at least 10uF of bypass capacitance is necessary.

Constant Drain Current vs. Constant Gate Voltage Operation

The AMM-11561CH pHEMT amplifier can be biased with a constant gate and drain voltage, or with a constant drain current by regulating the gate voltage. Using a constant gate and drain voltage reduces circuit complexity, but has variable current consumption during operation. However, regulating the gate voltage using feedback circuitry which controls the drain current to a constant value minimizes unit-to-unit variation in gain, output power, and compression points.

Under small signal excitation at a fixed temperature, these two approaches are equivalent because the current draw versus frequency is relatively constant in small signal. However, they will diverge in large signal conditions, where the drain current is affected by the input signal's frequency and power. The output power in saturation is relatively unchanged, as it is more strongly dependent on the drain voltage. However, output referred 1 dB compression point will decrease by 2-3 dB when operated with a constant drain current.

Die Mounting Recommendations

Mounting and Bonding Recommendations

Marki MMICs should be attached directly to a ground plane with conductive epoxy. The ground plane electrical impedance should be as low as practically possible. This willprevent resonances and permit the best possible electrical performance. Datasheetperformance is only guaranteed in an environment with a low electrical impedance ground.

Mounting - To epoxy the chip, apply a minimum amount of conductive epoxy to themounting surface so that a thin epoxy fillet is observed around the perimeter of the chip.Cure epoxy according to manufacturer instructions.

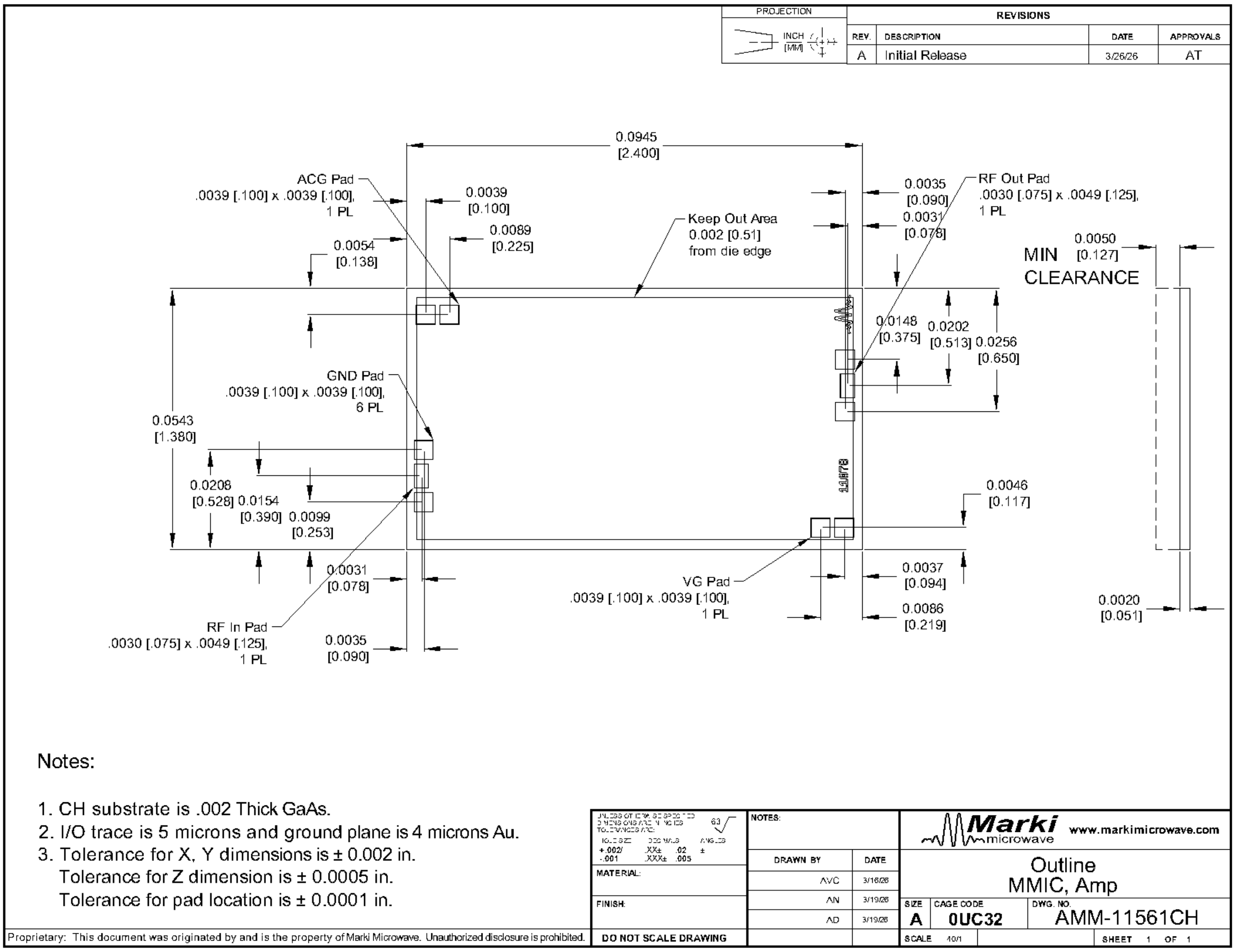
Wire Bonding - Ball or wedge bond with 0.025 mm (1 mil) diameter pure gold wire.Thermosonic wirebonding with a nominal stage temperature of 150 °C and a ball bondingforce of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Usethe minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should bestarted on the chip and terminated on the package or substrate. Bond wire inductancewill improve return loss. Bondwire inductance in the range of 30pH to 200pH will improveperformance.

Circuit Considerations – 50 Ω transmission lines should be used for all high frequencyconnections in and out of the chip. Wirebonds should be kept as short as possible, withmultiple wirebonds recommended for higher frequency connections to reduce parasiticinductance. In circumstances where the chip more than .001” thinner than thesubstrate, a heat spreading spacer tab is optional to further reduce bondwire length and parasitic inductance.

Mechanical Data

Outline Drawing

Download : Outline 2D Drawing



DISCLAIMER