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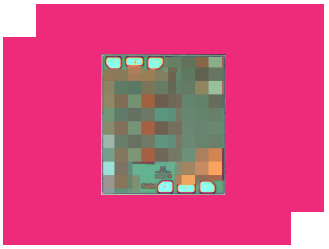
ADM-5931CH

Broadband Distributed Amplifier

DEVICE OVERVIEW

General Description

The ADM-5931CH is a broadband, power-efficient, moisture-resistant GaAs PHEMT distributed amplifier chip. The ADM-5931CH is designed to provide optimal LO drive for T3 mixers. Typically, it provides 11 dB of gain and +18 dBm saturated output power while requiring only 85 mA of current. T3 linearity is enhanced by ADM-5931's extended high frequency gain and lower even harmonic generation when compared to other distributed amplifiers in our catalog. It can be biased with internal circuitry, or with an external bias network for lower voltage and single supply operation. The enhanced moisture resistance process enables the bare chip to pass biased HAST testing without the use of a hermetically sealed package.



Features

- Low power consumption
- Optimized for use as a T3 LO buffer amplifier
- 2nd and 4th Harmonic Suppression
- 3rd and 5th Harmonic Generation
- Broadband 50 Ω Matching
- Unconditionally Stable
- Enhanced Moisture Resistance

Applications

- Amplification Clock Signals
- Electronic Warfare
- Test and Measurement Equipment

Functional Block Diagram

N/A

Part Ordering Options

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
ADM-5931CH	Broadband Distributed Amplifier	CH	REACH RoHS	Released	EAR99

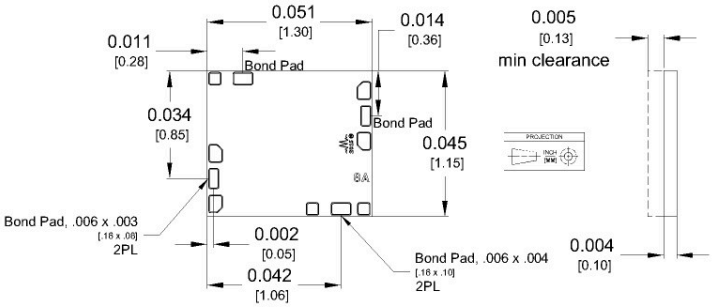
Table Of Contents

Revision History

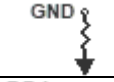
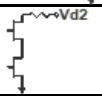
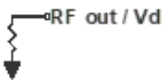
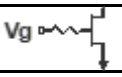
Revision Code	Revision Date	Comment
-	2018-01-01	Datasheet initial Release
A	2019-07-01	Thermal Resistance Spec Corrected
B	2020-12-01	Added Max Junction Temperature Specification

Port Configuration and Functions

Port Diagram



Port Functions

Port	Function	Description	DC Equivalent Circuit
GND	Gnd	Back of chip should be connected to RF/DC ground with low electrical and thermal resistance.	
RF In	RF Input	This pin is DC coupled and matched to 50 Ω.	
Vd2	Vd2	Optional drain bias port. External decoupling capacitors are required.	
Vd/RF Out	Vd / RF Out	This pad is DC coupled and matched to 50 Ω.	
Vg	Vg	Gate control for the amplifier. External decoupling capacitors are required.	

Specifications

Absolute Maximum Ratings

Parameter	Maximum Rating	Unit
Input Power	20	dBm
Maximum Operating Temperature	85	°C
Maximum Storage Temperature	150	°C
Max Junction Temperature to Maintain 10^6 Hours Mean Time to Failure (MTTF):	175	°C
Minimum Operating Temperature	-55	°C
Minimum Storage Temperature	-65	°C
Negative Bias Current	2	mA
Negative Bias Voltage	-0.3	V
Positive Bias Current	150	mA
Positive Bias Voltage	9	V
Power Dissipation	2	W
Thermal Resistance	67	°C/W

Package Information

Parameter	Details	Rating
ESD	< 250 Volts	HBM Class 0
Dimensions	-	1.30 x 1.15 mm

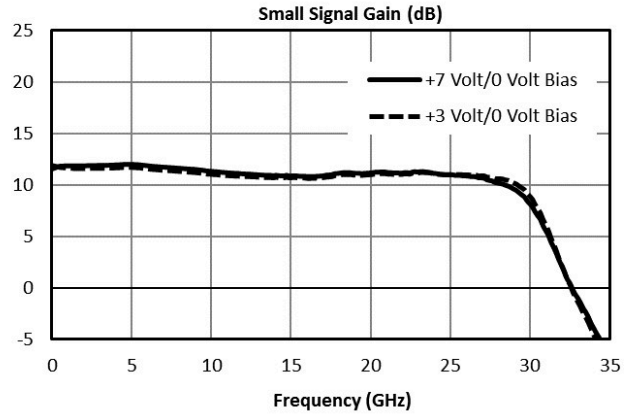
Electrical Specifications

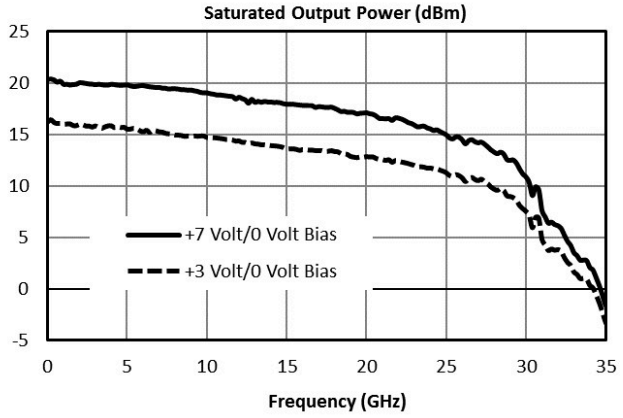
Specifications measured in a 50-Ohm system.

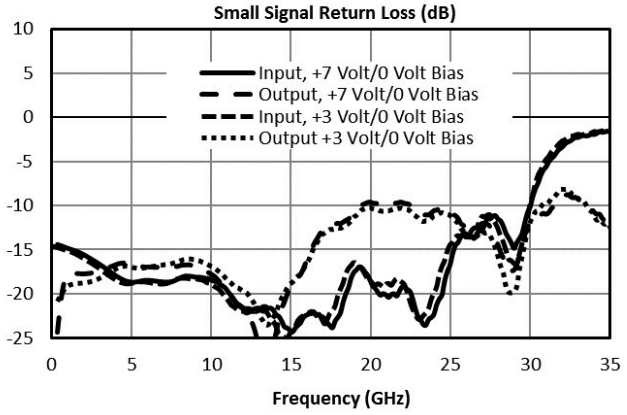
Parameter	Test Conditions	Minimum Frequency (GHz)	Maximum Frequency (GHz)	Min	Typ	Max	Unit
Current Consumption	Vd: +5.0 to +7.0 (External) Vg: -0.25 Volts	0	28	-	85	-	mA
Current Consumption	Vd: +5.0 to +7.0 (External) Vg: 0 Volts	0	28	-	120	-	mA
Input for Saturated Output	-	0	28	-	8	-	dBm
Input Return Loss	-	0	28	-	16	-	dB
Noise Figure	-	0	28	-	6	-	dB
Output IP3	-	0	28	-	27	-	dBm
Output P1dB	-	0	28	-	16	-	dBm
Output Power	With Negative Bias	0	28	-	18	-	dBm
Output Return Loss	-	0	28	-	14	-	dB
Phase Noise @ 10 kHz Offset	-	0	28	-	-153	-	dBc/Hz
Small Signal Gain	With Negative Bias	0	28	-	11	-	dB

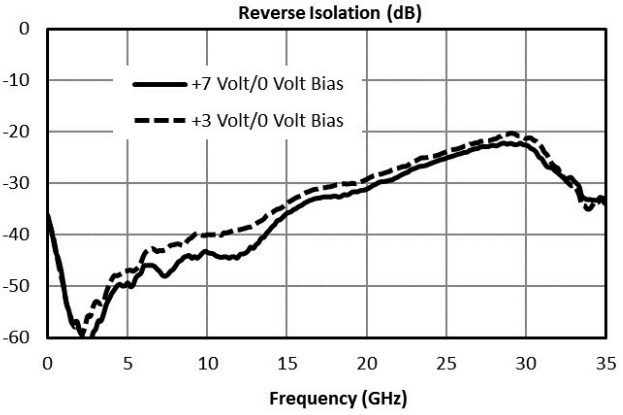
Positive Only (+3, +7V) Bias (Bias tee on RF output), Grounded Gate (Bias tee on RF input)

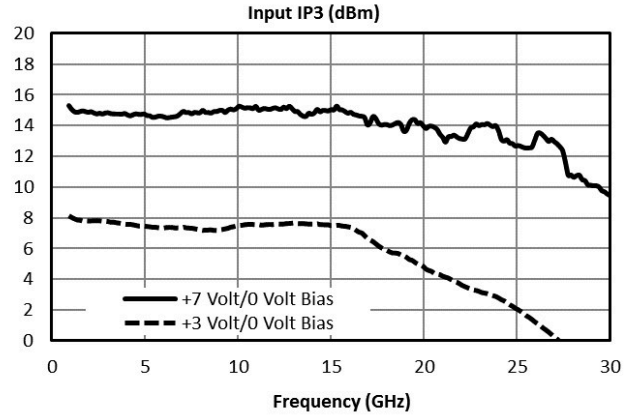
Typical Performance Plots

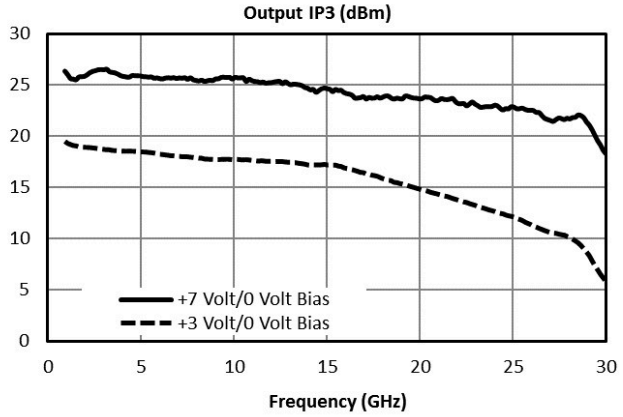


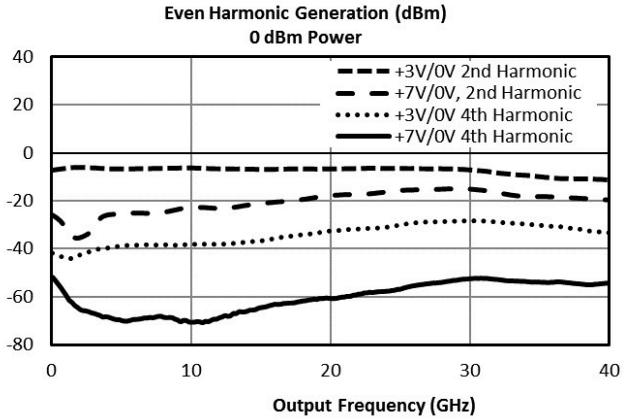


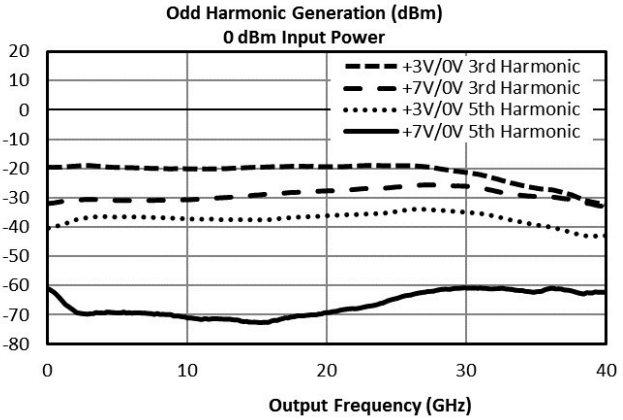




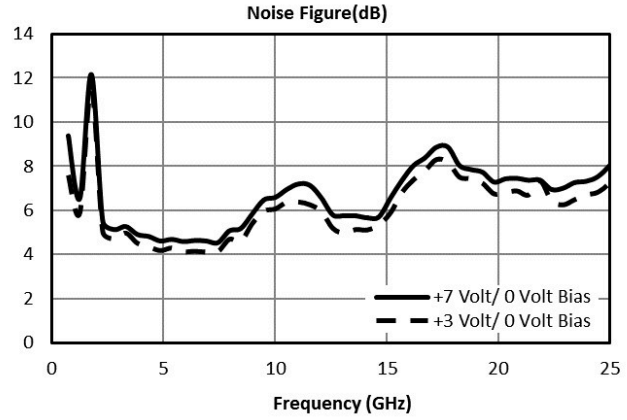




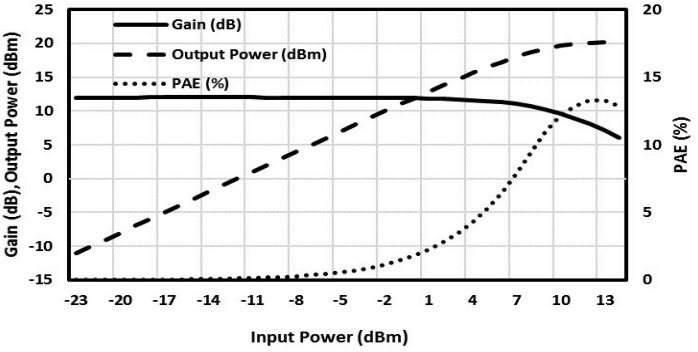




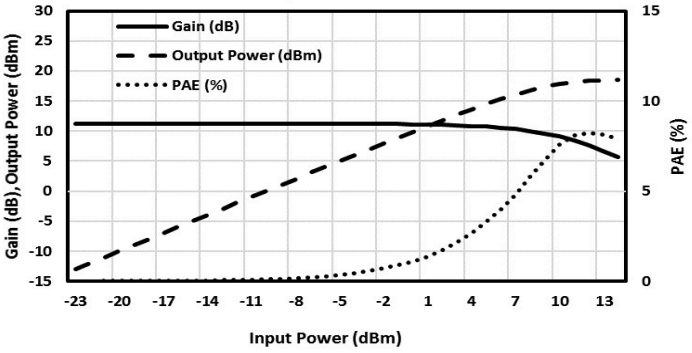
Noise Figure(dB)



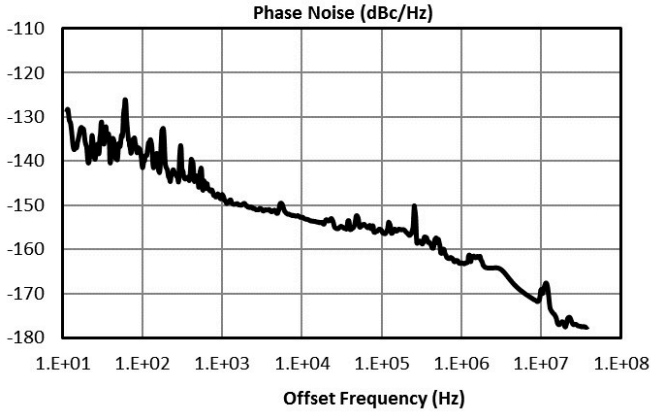
Gain, Output Power, PAE vs. Input Power @ 8.6 GHz, 7V 0 V Bias



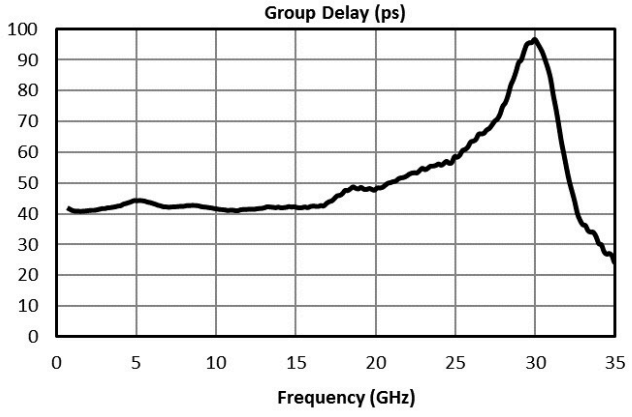
Gain, Output Power, PAE vs. Input Power @ 17.25 GHz, 7V 0 V Bias



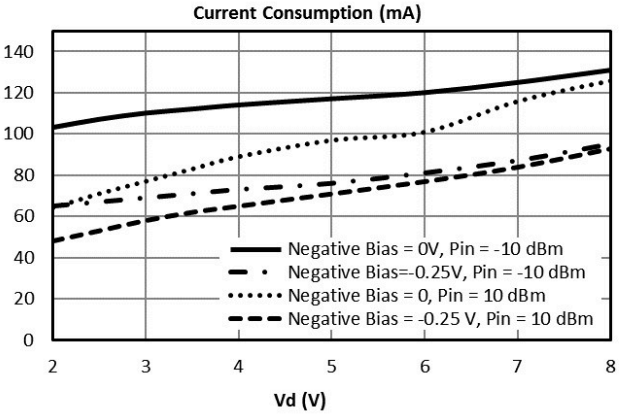
Phase Noise (dBc/Hz)



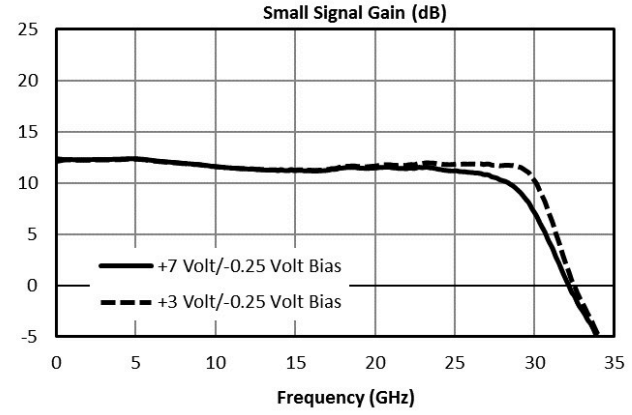
Group Delay (ps)



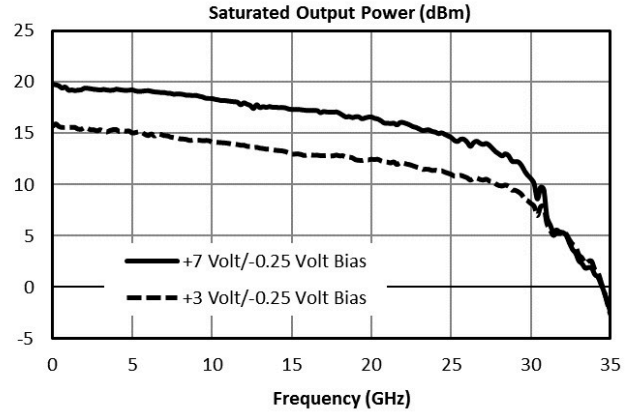
Current Consumption (mA)

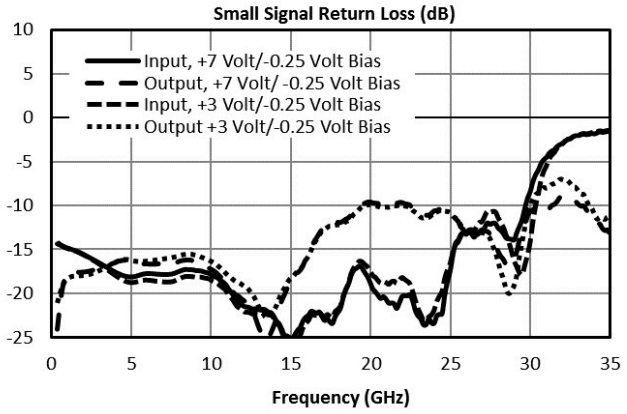


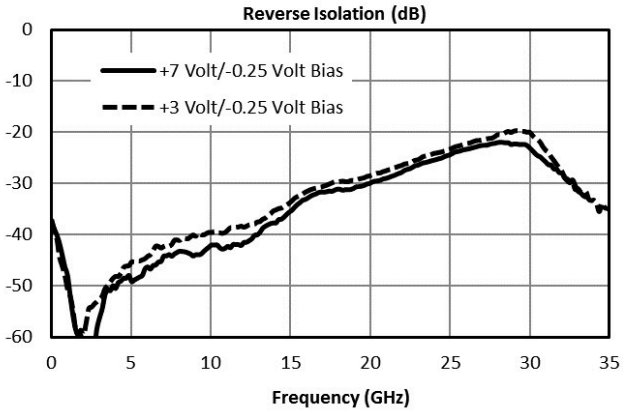
Small Signal Gain (dB)

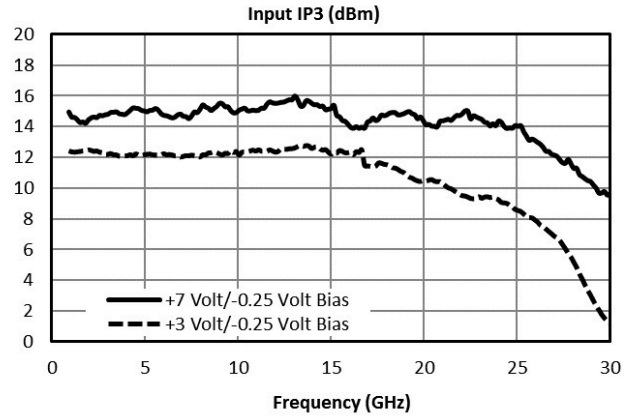


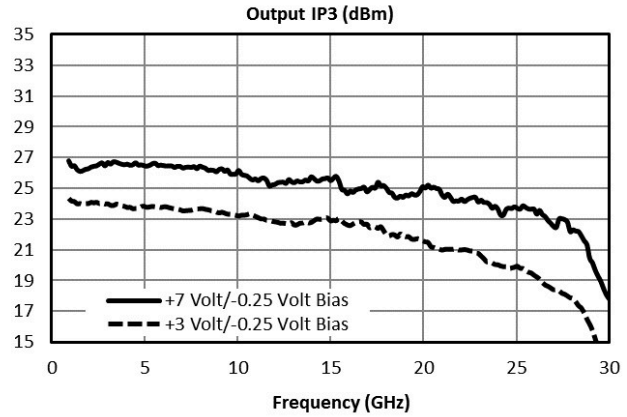
Saturated Output Power (dBm)

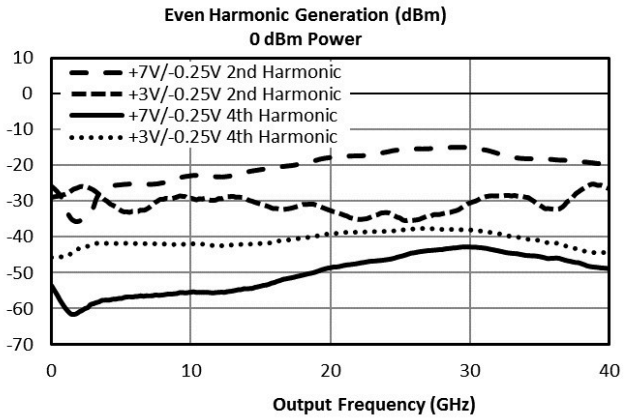


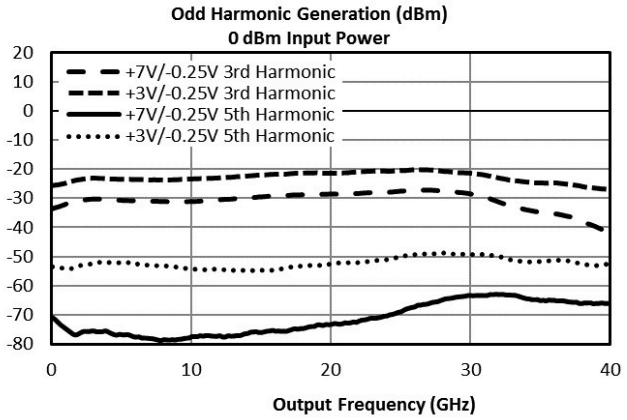


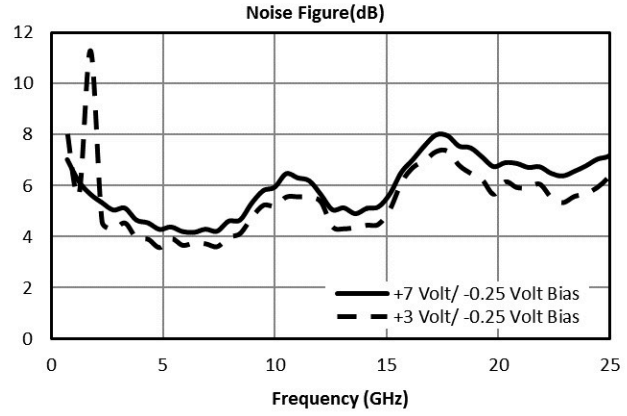


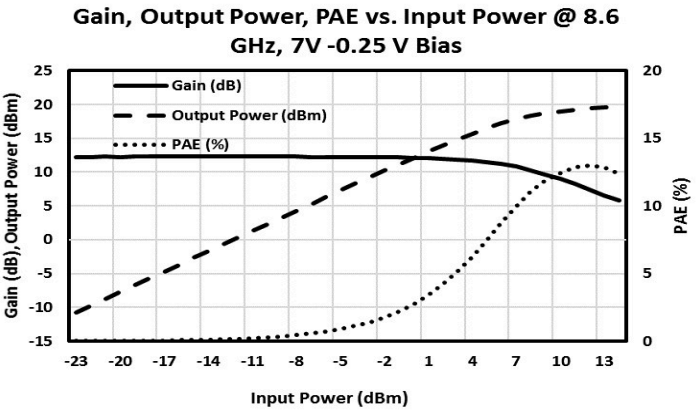


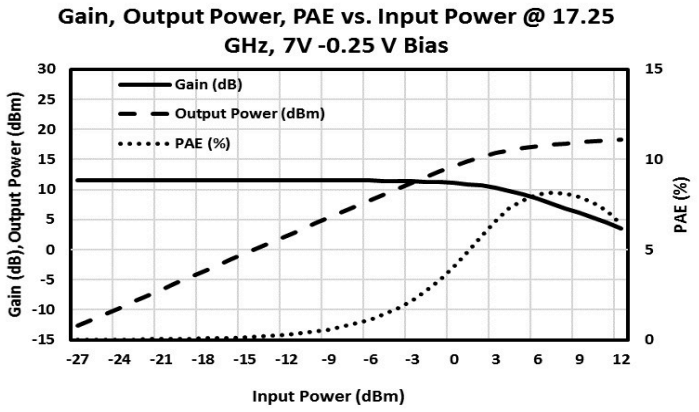












Application Information

Biasing and Operation

RF In / RF Out – Input and output signals should be connected by 50 ohm microstrip or coplanar traces to well matched 50 ohm sources and loads. DC blocking capacitors and bias tees are required.

Vg – Negative gate voltage is optional to improve lifetime of the amplifier and reduce current consumption. Harmonic generation is also significantly affected by the negative gate voltage level. It may be supplied through the Vg pad or through the RF input pad using an external bias tee

Vd- It is recommended that bias voltage Vd is applied through a bias tee on the RF output, but bias supply can also be supplied to Vd through Vd2 pad if desired. This will result in increased operating temperature and slightly reduced gain and power output. Bias supply should be voltage limited below 9 V and current limited below 150 mA at all times. The operational bias voltage should be between 3 V and 7 V for full small-signal gain, or between 5 V and 7 V for full gain, linearity and power output. If bias tee on RF output is used, pad Vd2 voltage should be left unconnected (not grounded).

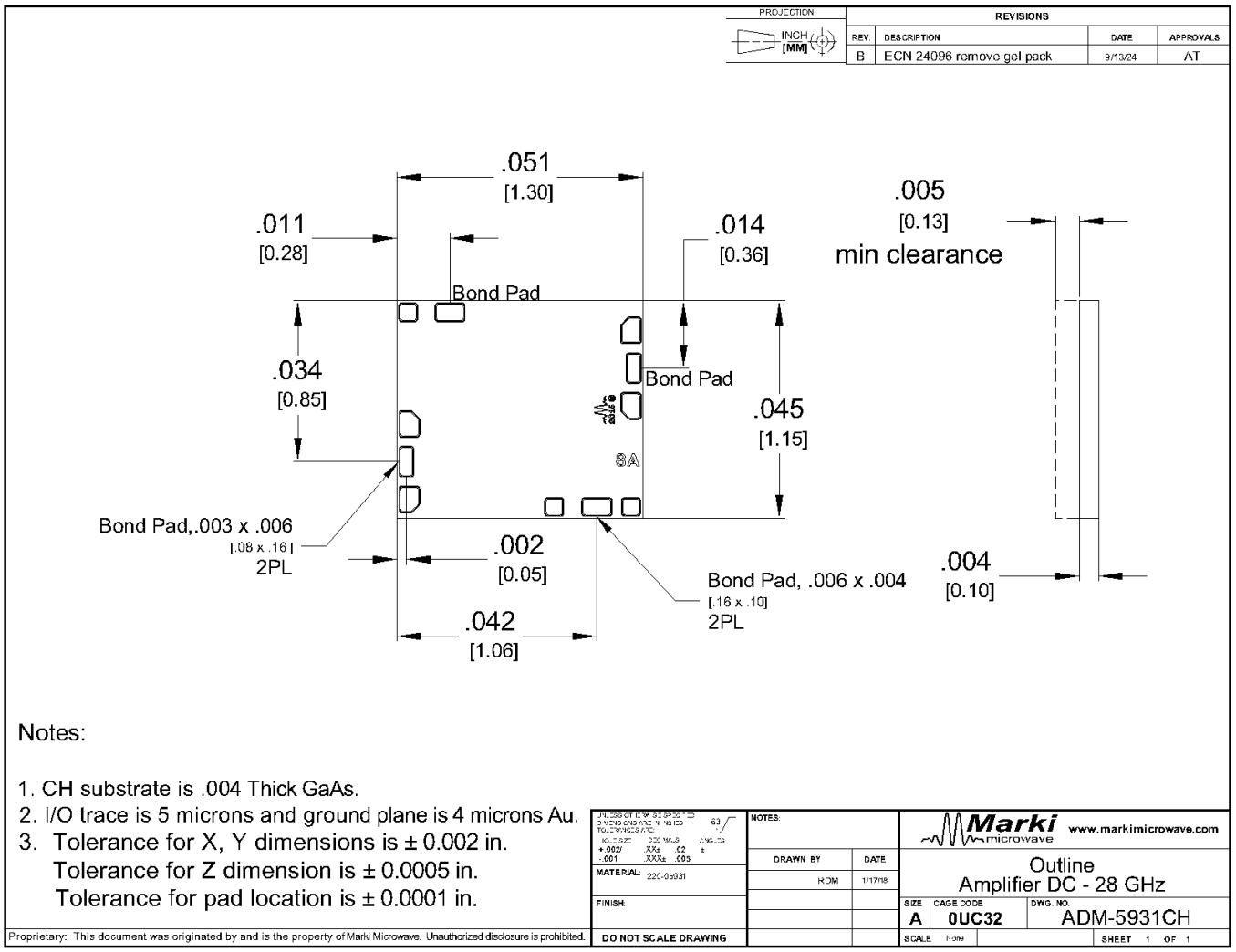
Bias Circuitry – The capacitors on the Vd and Vg lines prevent low frequency oscillation. They may be reduced or omitted in bias circuits with sufficient low-frequency loss. Designers are encouraged to experiment if they want to modify or omit the bias circuitry.

DC/RF Ground – The back of the chip should be connected to a low noise RF and DC ground with very low electrical and thermal resistance for high frequency operation and thermal heat sinking.

Mechanical Data

Outline Drawing

Download : Outline 2D Drawing



Notes

GaAs MMIC devices are susceptible to Electrostatic Discharge. Use proper ESD precautions when handling these items.

DISCLAIMER