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Sales & Customer Support: sales@markimicrowave.com
Tech Support: support@markimicrowave.com

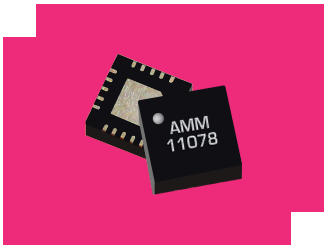
AMM-11078PSM

0.01 - 40 GHz Surface Mount Amplifier

DEVICE OVERVIEW

General Description

The AMM-11078PSM is a wideband GaAs distributed amplifier covering 0.01 to 40 GHz, delivering 17.2 dB small-signal gain with high output power and linearity. It provides up to +23.5 dBm saturated output power, with output IP3 up to +32.5 dBm. Operating from a +7V supply at 205 mA typical current, the amplifier is internally matched to 50 Ω at both the RF input and output ports. These features make it well-suited for wideband driver stages in RF/mmWave front ends, test and measurement instrumentation, electronic warfare, and general-purpose broadband gain block applications.



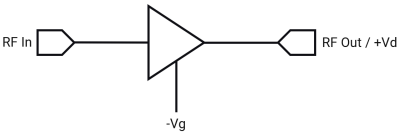
Features

- High Frequency Wideband Operation
- High Saturated Output Power, +23.5 dBm Typical
- Low Noise Figure, 3.3 dB Typical
- Positive Gain Slope

Applications

- Satellite Communications
- Test and Measurement Equipment
- Electronic Warfare
- 5G Transceivers

Functional Block Diagram



Part Ordering Options

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
AMM-11078PSM	0.01 - 40 GHz Surface Mount Amplifier	QFN	REACH RoHS	Released	3A001.b.2.d
EVB-AMM-11078P	Evaluation Board, 0.01-40GHz Surface Mount Amplifier	EVB	REACH RoHS	Released	3A001.b.2.d

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Table Of Contents

Revision History

Revision Code	Revision Date	Comment
-	2026-07-22	Initial Release

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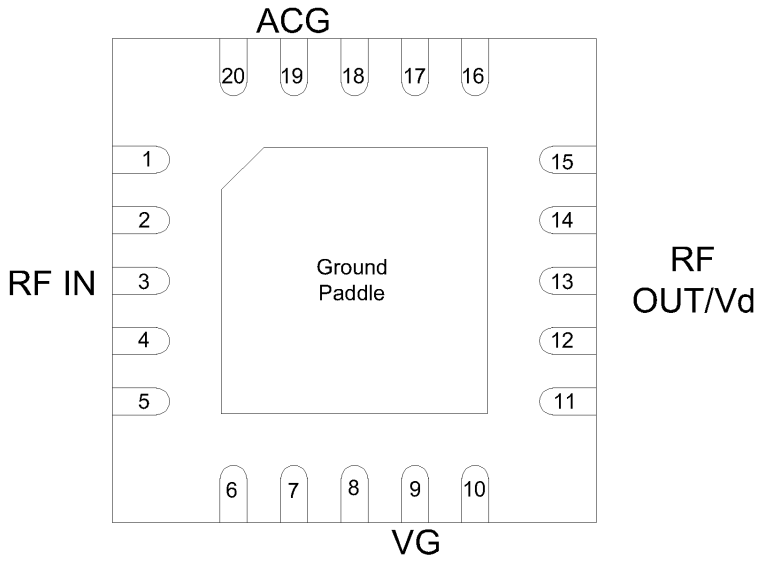
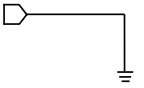
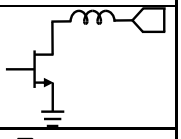
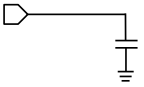
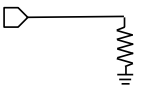
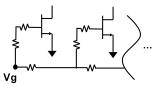
Port Configuration and Functions

Port Diagram

A port diagram of the AMM-11078PSM QFN package is shown below (X-ray view from the top).



Port Functions

Port	Function	Description	DC Equivalent Circuit
GND	Ground	IC backside must be connected to a DC/RF ground with high thermal and electrical conductivity.	
Pin 13	RF Out / Vd	The RF Out/ Vd pin supplies DC voltage to the drain of the amplifier and also acts as the RF output. This pin requires an external bias-tee.	
Pin 19	ACG	The ACG pin provides additional off chip bypass capacitance. A 0.1uF chip capacitor is recommended.	
Pin 3	RF Input	This is the RF input port of the device, and is RF matched to 50 Ω and requires a DC blocking capacitor.	
Pin 9	Vg	Gate control for the amplifier. The user should apply between -0.15V and -0.35V to Vg pin before applying positive DC voltage to any Vd port. Lower (more negative) voltages on a Vg pin will result in lower drain current and lower small signal gain.	

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Specifications

Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If any one of these limits are exceeded, the device may become inoperable or have a reduced lifetime.

Parameter	Maximum Rating	Unit
Drain Current (RF Applied)	550	mA
Drain Supply Voltage (Vd)	10	V
Gate Voltage (Vg)	-0.5	V
Maximum Operating Temperature for MTTF > 1E6 hours	85	°C
Maximum Storage Temperature	150	°C
Max Junction Temperature for MTTF > 1E6 Hours	175	°C
Max Power Dissipation for MTTF of 1E6 hours at 85°C Baseplate Temperature	3.9	W
Minimum Operating Temperature for MTTF > 1E6 hours	-55	°C
Minimum Storage Temperature	-65	°C
RF Input Power	18	dBm
θ_Jc, Junction to Case Thermal Resistance	23	°C/W

Package Information

Parameter	Details	Rating
ESD	< 250 Volts	HBM Class 0
Dimensions	-	4 x 4 mm
Moisture Sensitivity Level	-	MSL 1

Recommended Operating Conditions

The Recommended Operating Conditions indicate the limits, inside which the device should be operated, to guarantee the performance given in Electrical Specifications Operating outside these limits may not necessarily cause damage to the device, but the performance may degrade outside the limits of the electrical specifications. For limits, above which damage may occur, see Absolute Maximum Ratings. Power Supply DC current should be modified by changing bias voltage Vg to maintain junction temperature within MTTF target for given operating conditions.

Parameter	Min	Nominal	Max	Unit
Ambient Temperature	-40	25	85	°C
Power Supply DC Voltage	4	7	8	V
Power Supply DC Current (Id) (No RF Input)	150	205	220	mA
Negative Bias Voltage (Vg)	-0.35	-0.25	-0.15	V
Input Power for Saturation	10	11	15	dBm

Sequencing Requirements

Turn-on Procedure:
1. Apply negative bias to Vg
2. Apply Vd

Turn-off Procedure:
1. Turn off Vd
2. Turn off Vg

Note: RF input power can be injected at any moment in the bias sequencing procedure.

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Electrical Specifications

Unless otherwise specified, electrical specifications apply at TA=+25°C, Vd = 7 V, Vg set as required to achieve Id = 205 mA in a 50 Ω system.

Parameter	Test Conditions	Minimum Frequency (GHz)	Maximum Frequency (GHz)	Min	Typ	Max	Unit
Small Signal Gain	Pin = -15 dBm	0.01	40	-	17.2	-	dB
Input Return Loss	Pin = -15 dBm	0.01	40	-	17	-	dB
Output Return Loss	Pin = -15 dBm	0.01	40	-	20	-	dB
Reverse Isolation	Pin = -15 dBm	0.01	40	-	20	-	dB
Psat	Pin = 11 dBm	0.01	40	-	23.46	-	dBm
Input P1dB	-	0.01	40	-	5	-	dBm
Output P1dB	-	0.01	40	-	21.5	-	dBm
Input IP3	Pin -8 dBm, 1 MHz Tone Spacing	0.01	40	-	15	-	dBm
Output IP3	Pin -8 dBm, 1 MHz Tone Spacing	0.01	40	-	32.5	-	dBm
Input IP2	Pin -8 dBm, 1 MHz Tone Spacing	0.01	40	-	19.5	-	dBm
Output IP2	Pin -8 dBm, 1 MHz Tone Spacing	0.01	40	-	36.5	-	dBm
Noise Figure	Pin = -15 dBm	0.01	40	-	3.3	-	dB
Current Consumption	-	0.01	40	-	205	-	mA

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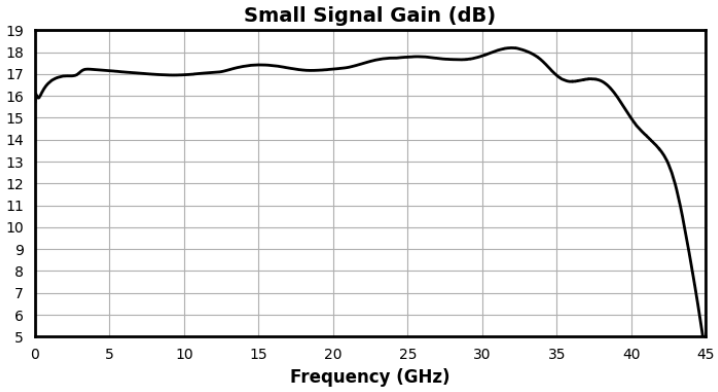
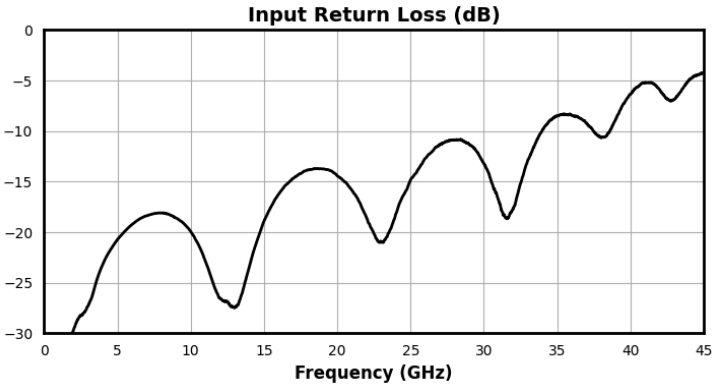
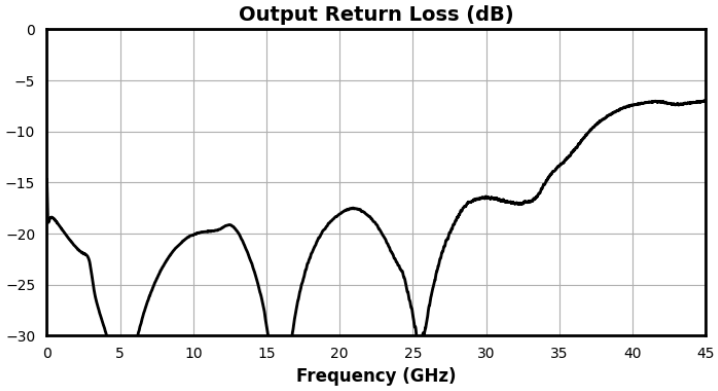
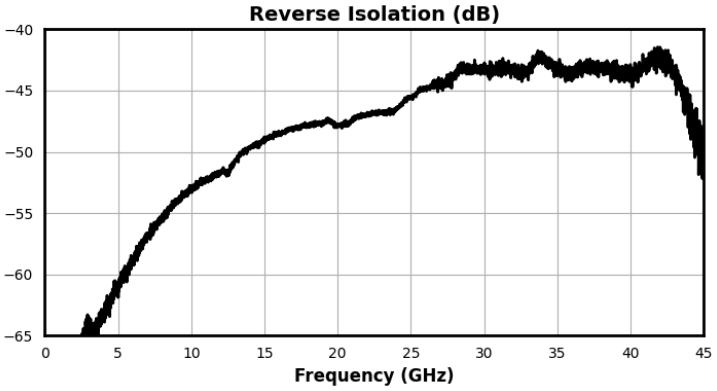
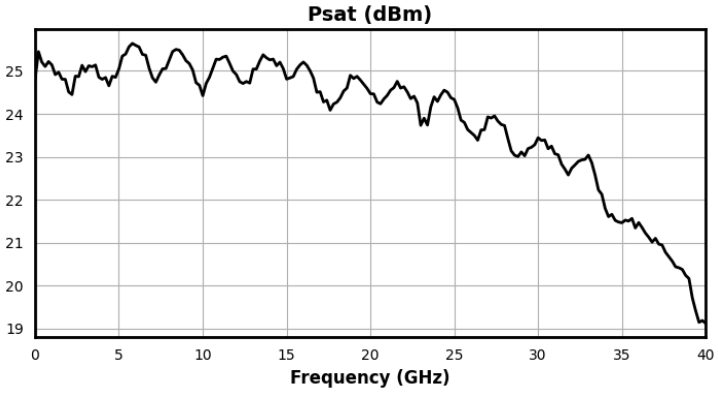
Typical Performance Plot

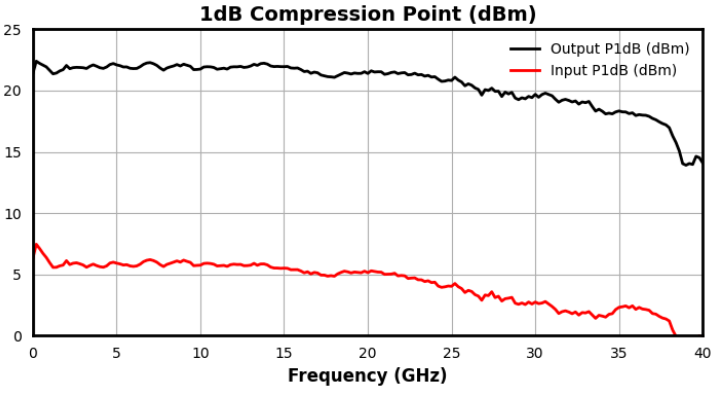


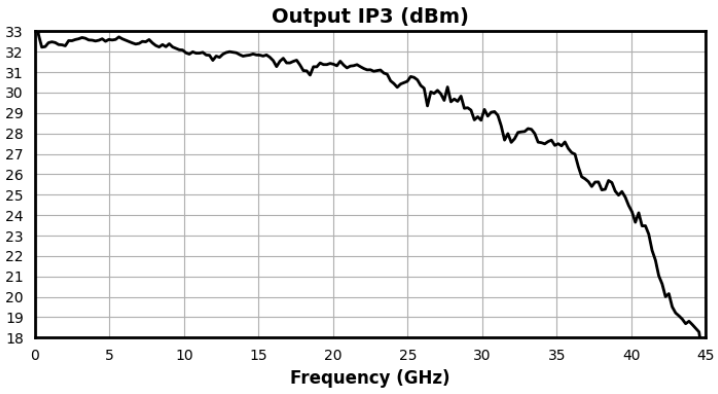


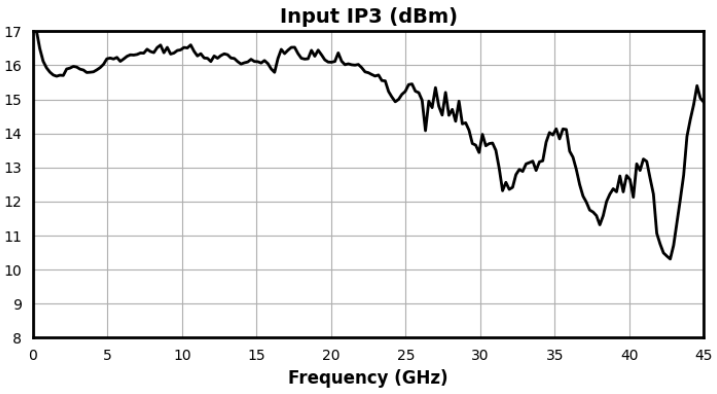












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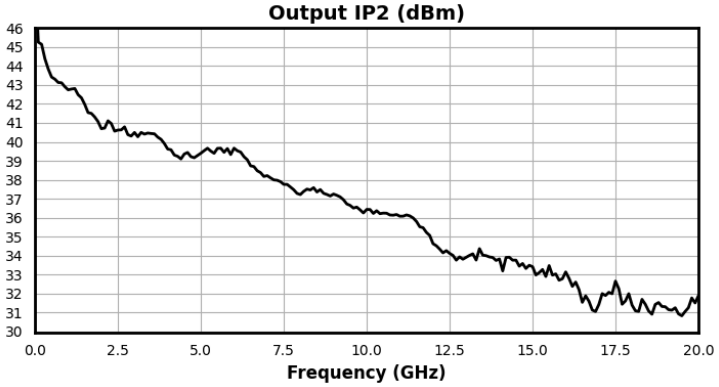

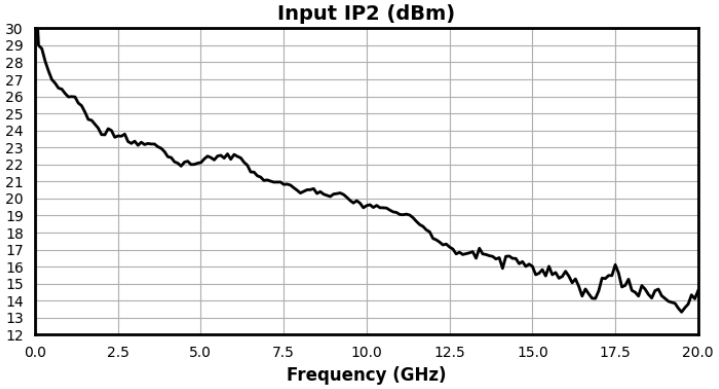

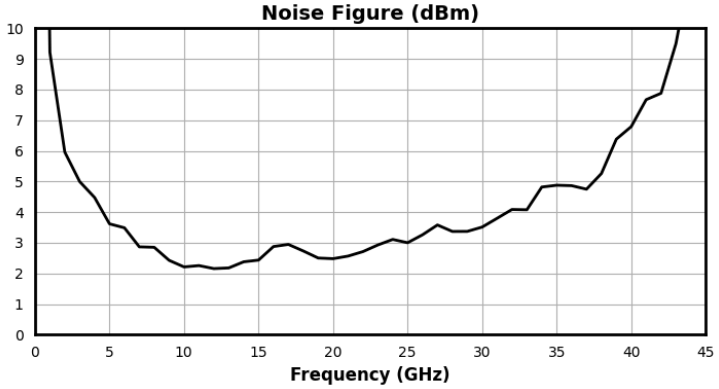

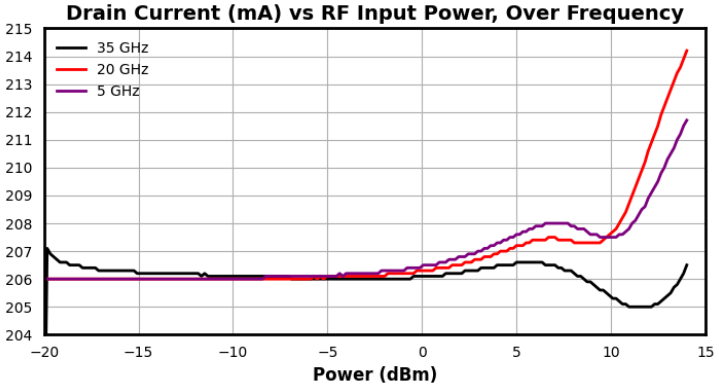

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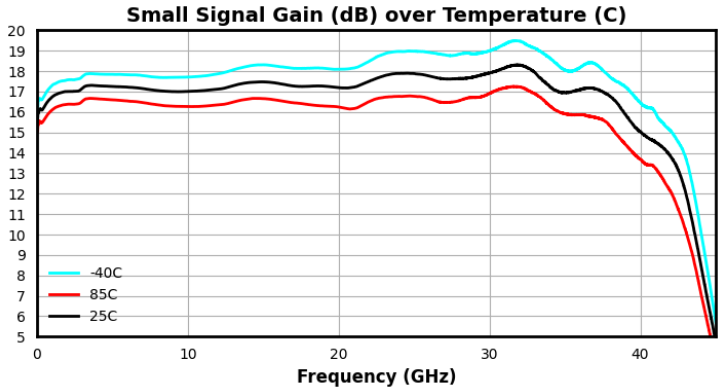
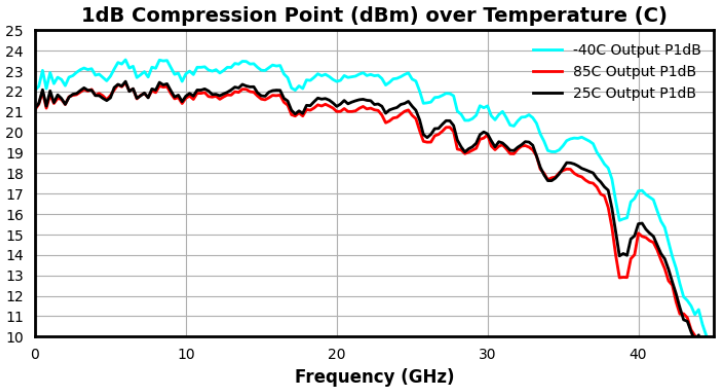
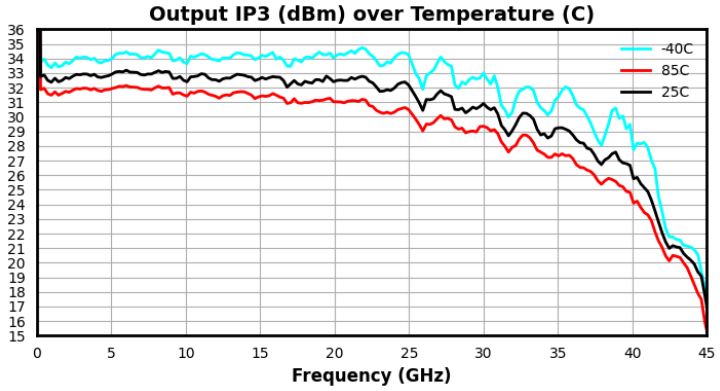
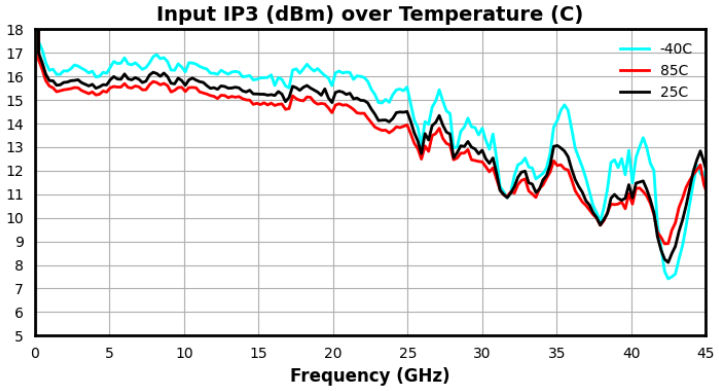
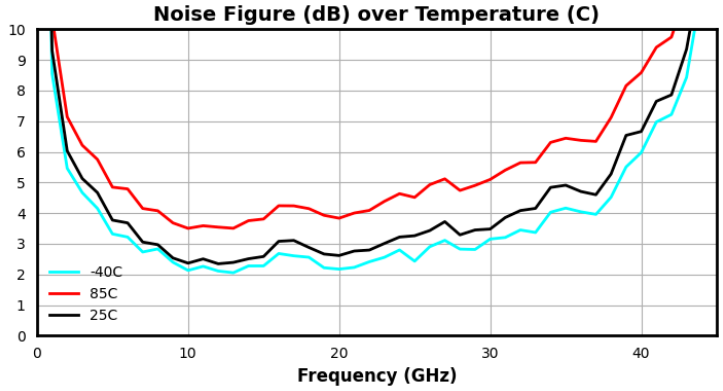
Typical Performance Plots (vs Temperature)

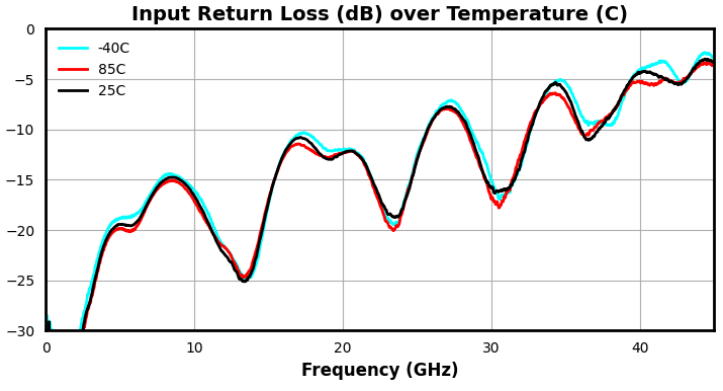


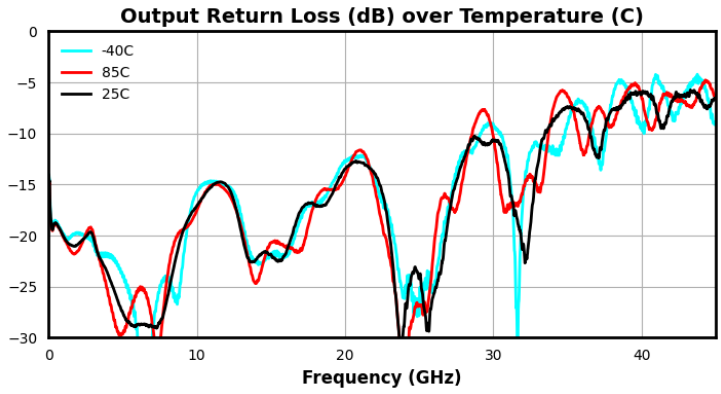


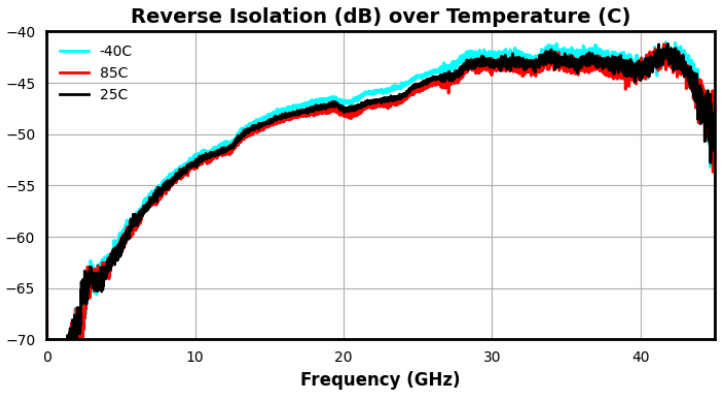












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Application Information

Below are the recommended application circuits for the AMM-11078PSM. This application circuit is used for the performance plots shown in this datasheet. However, each PCB layout and environment are different which may require minor modifications of the biasing network. Recommend use with Marki Bias Tee.

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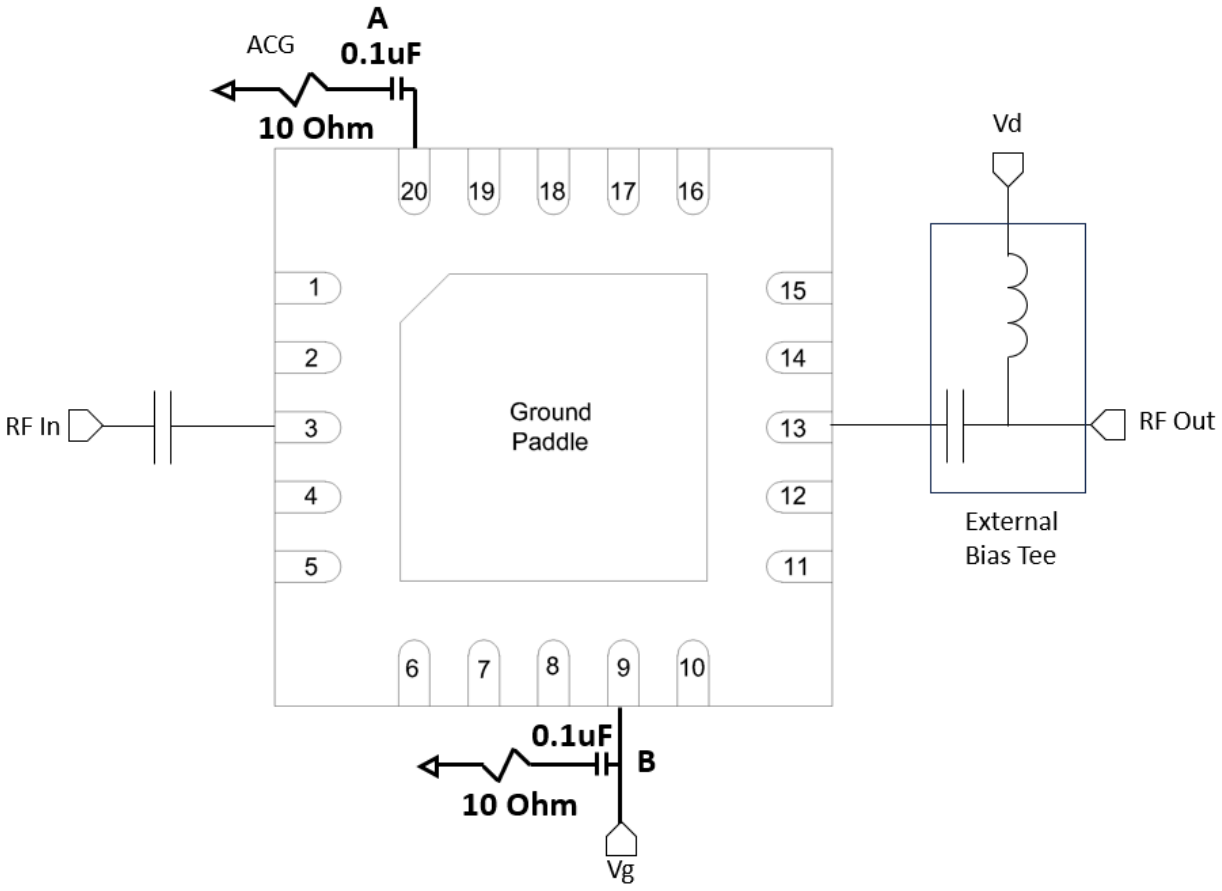
Application Circuit



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Application Circuit Description

Low Frequency Operation

The AMM-11078 can be used at low frequency approaching DC. Operation below 10MHz requires using larger bypass capacitors to provide AC ground across the frequency range of interest. It is recommended to place additional bypass capacitance in parallel with designator **A**. For example, if operation is desired to 100KHz at least 10uF of bypass capacitance is necessary.

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Constant Drain Current vs. Constant Gate Voltage Operation

The AMM-11078 pHEMT amplifier can be biased with a constant gate and drain voltage, or with a constant drain current by regulating the gate voltage. Using a constant gate and drain voltage reduces circuit complexity, but has variable current consumption during operation. However, regulating the gate voltage using feedback circuitry which controls the drain current to a constant value minimizes unit-to-unit variation in gain, output power, and compression points.

Under small signal excitation at a fixed temperature, these two approaches are equivalent because the current draw versus frequency is relatively constant in small signal. However, they will diverge in large signal conditions, where the drain current is affected the input signal's frequency and power. The output power in saturation is relatively unchanged, as it is more strongly dependent on the drain voltage. However, output referred 1 dB compression point will decrease by 2-3 dB when operated with a constant drain current.

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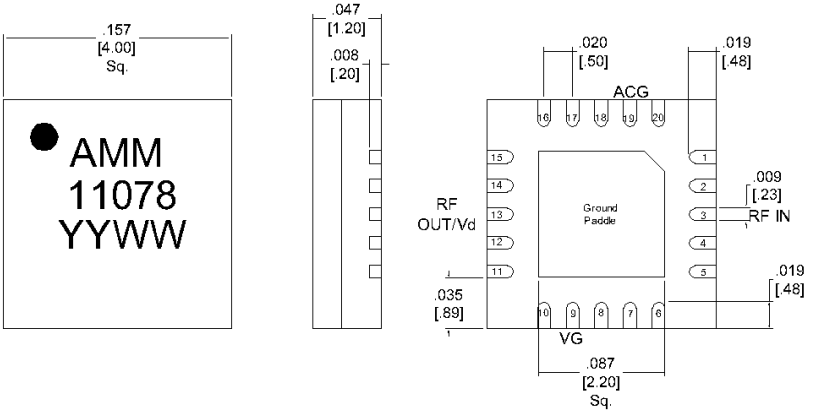
Mechanical Data

Outline Drawing

Download : Outline 2D Drawing



Pin #	Function
1	GND
2	GND
3	RF IN
4	GND
5	GND
6	GND
7	GND
8	GND
9	VG
10	GND
11	GND
12	GND
13	RF OUT/Vd
14	GND
15	GND
16	GND
17	GND
18	GND
19	ACG
20	GND

Notes (unless otherwise specified):

1. Substrate material is LCP.
2. I/O Leads and Die Paddle is (from base to finish):
   Ni: 0.5um MIN
   Pd: 0.02um MIN
   Au: 0.05um MAX
3. All unconnected pins should be connected to PCB RF ground.

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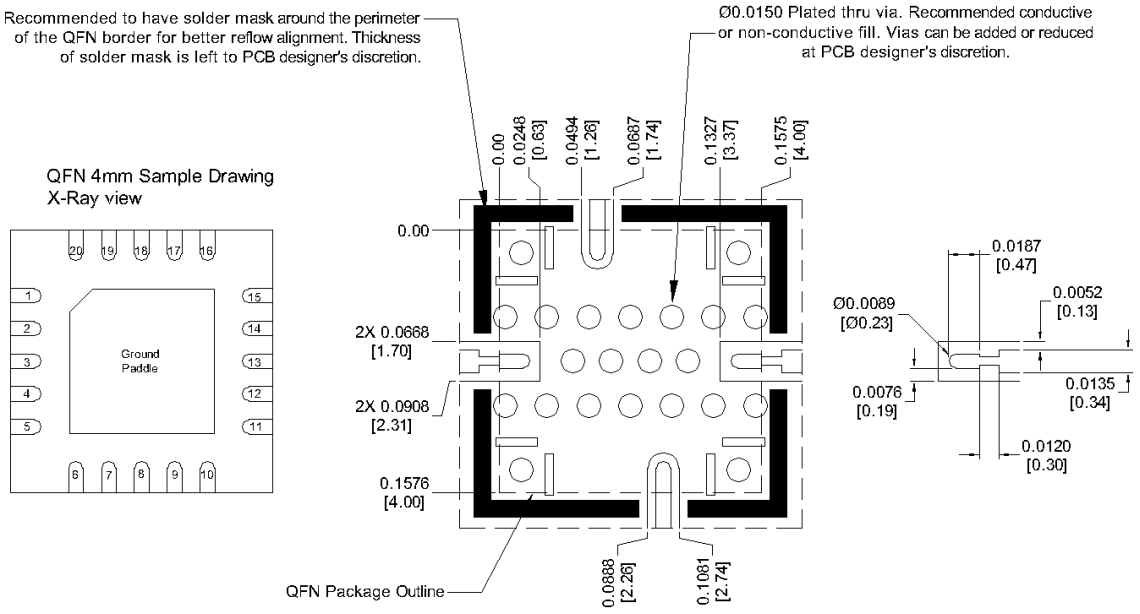
Footprint Image

Download : Footprint Drawing

Pin #	Function
1	GND
2	GND
3	RF IN
4	GND
5	GND
6	GND
7	GND
8	GND
9	VG
10	GND
11	GND
12	GND
13	RF OUT/Vd
14	GND
15	GND
16	GND
17	GND
18	GND
19	ACG
20	GND



The Landing Pattern is to be used on Rogers 4003, 0.008" thick $\frac{1}{2}$ Oz Copper both sides.

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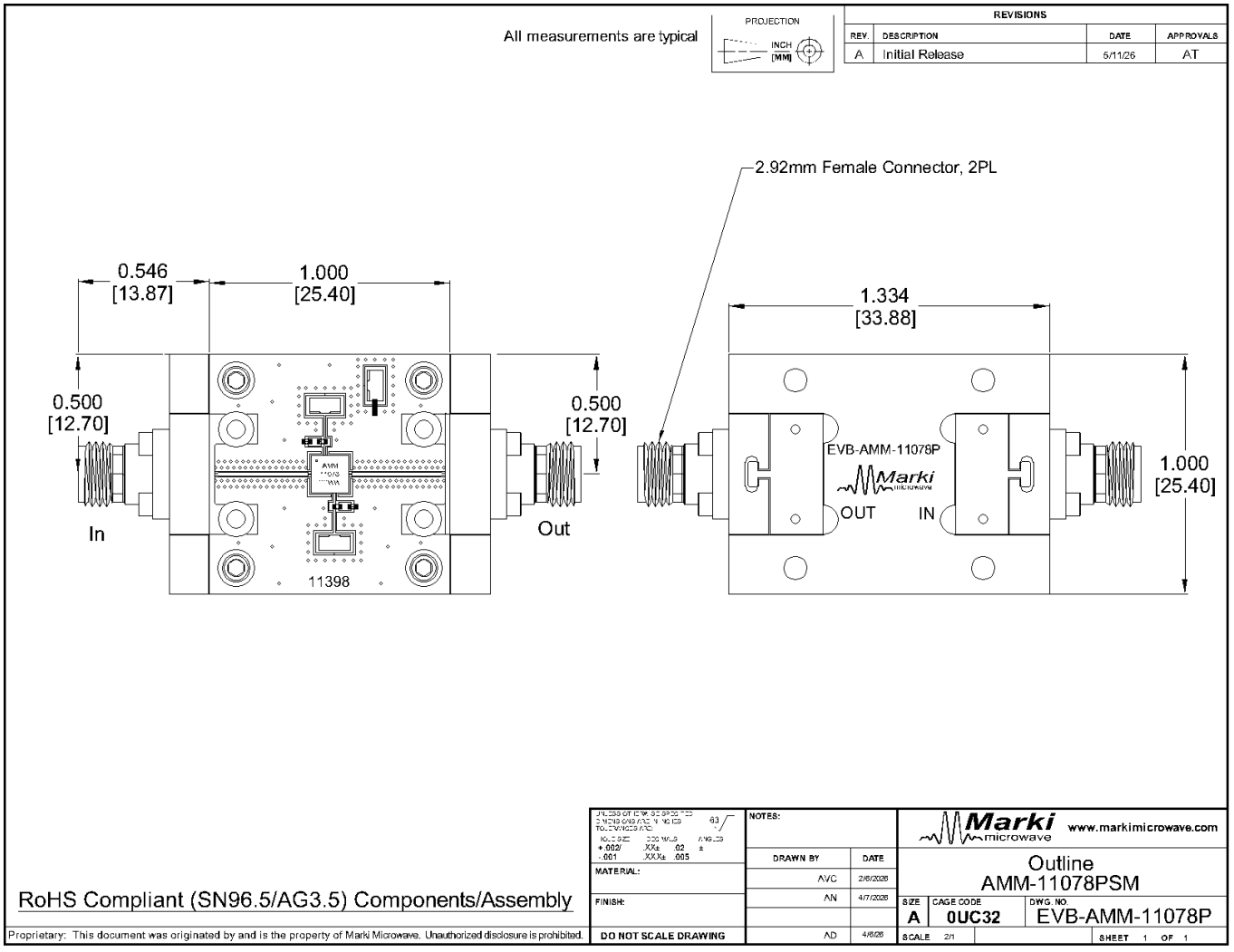
Evaluation Board - Outline Drawing



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