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Sales & Customer Support: sales@markimicrowave.com
Tech Support: support@markimicrowave.com

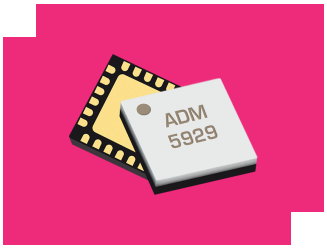
ADM-0026-5929SM

Broadband Distributed Amplifier

DEVICE OVERVIEW

General Description

The ADM-0026-5929SM is a broadband, efficient GaAs PHEMT distributed amplifier in a 4mm QFN surface mount package. It is designed to provide optimal LO drive for T3 mixers and offers 13 dB typical gain and 20 dBm typical saturated output power for 165 mA of current. Extended high frequency gain offers improved harmonic generation and rise times improving T3 linearity. The ADM-0026-5929SM is biased with a 5-7 volt positive bias and an optional current reducing negative voltage with external bias tee. The ADM-0026-5929SM is an excellent alternative to competing GaAs PHEMT distributed amplifiers.



Download s-parameters here

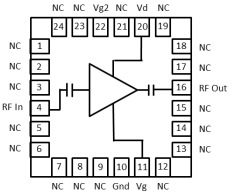
Features

- Fast <10 ps risetime
- 3rd and 5th Harmonic Generation
- Broadband 50 Ω Matching
- Unconditionally Stable

Applications

- Amplification Clock Signals
- Electronic Warfare
- Test and Measurement Equipment

Functional Block Diagram



Part Ordering Options

Part Number	Description	Package	Packing Size	Green Status	Product Lifecycle	Export Classification
ADM-0026-5929SM	Broadband Distributed Amplifier	QFN	-	REACH RoHS	Released	EAR99
EVAL-ADM-5929SM	Evaluation Board, Broadband Distributed 26.5 GHz Amplifier	EVAL	-	REACH RoHS	Released	EAR99
ADM-0026-5929TR	Tape and Reel, Broadband Distributed Amplifier	QFN	7"	REACH RoHS	Released	EAR99

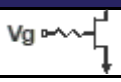
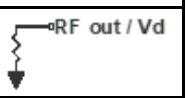
Table Of Contents

Revision History

Revision Code	Revision Date	Comment
-	2015-01-01	Datasheet Initial Release
A	2019-10-01	Plating call-out is now ENEPIG effective starting on D/C 1846

Port Configuration and Functions

Port Functions

Port	Function	Description	DC Equivalent Circuit
11	Vg	Gate control for the amplifier. External decoupling resistor/capacitor is required.	
1-3, 5-10, 12-15, 17-20, 22, 24	NC	These pins are not connected internally. Datasheet performance is tested with NC pins grounded.	-
16	RF Out / Vd	This pad is DC coupled and matched to 50 Ω.	
21	Vd2	External decoupling resistor/capacitor is required.	
4	RF Input	This pin is DC coupled and matched to 50 Ω.	
Paddle	Gnd	Ground pad should be connected to RF/DC ground with low electrical and thermal resistance.	-

Specifications

Absolute Maximum Ratings

Parameter	Maximum Rating	Unit
Maximum Operating Temperature	85	°C
Maximum Storage Temperature	150	°C
Minimum Operating Temperature	-55	°C
Minimum Storage Temperature	-65	°C
Negative Bias Current	2	mA
Negative Bias Voltage	-2	V
Positive Bias Current	275	mA
Positive Bias Voltage	9	V
Power Dissipation	2	W
RF Input Power	20	dBm
Thermal Resistance	0.873	°C/W

Package Information

Parameter	Details	Rating
ESD	< 250 Volts	HBM Class 0
Dimensions	-	4 x 4 mm
Moisture Sensitivity Level	-	MSL 1

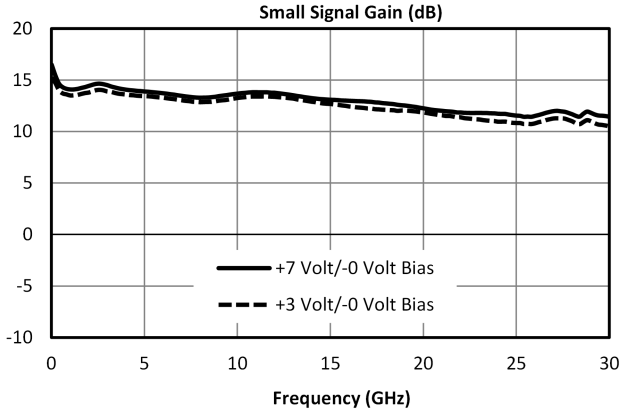
Electrical Specifications

Specifications measured in a 50-Ohm system.

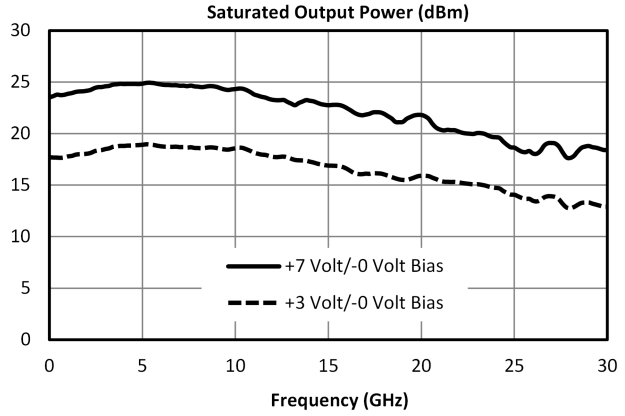
Parameter	Test Conditions	Minimum Frequency (GHz)	Maximum Frequency (GHz)	Min	Typ	Max	Unit
Bias Requirements, External	Vd: +5.0 to +7.0 Vg: -0.25 Volts	0	26.5	-	165	-	mA
Bias Requirements, External	Vd: +5.0 to +7.0 Vg: 0 Volts	0	26.5	-	225	-	mA
Input for Saturated Output	-	0	26.5	5	10	12	dBm
Noise Figure	-	0	26.5	-	5.5	-	dB
Output IP3	-	0	26.5	-	26	-	dBm
Output P1dB	-	0	26.5	-	15	-	dBm
Output Power	With Negative Bias	0	26.5	-	20	-	dBm
Return Loss	-	0	26.5	-	14	-	dB
Small Signal Gain	With Negative Bias	0	26.5	-	13	-	dB

Typical Performance Plots - Positive Only (+3 to +7V) Bias (Pin 16 Output), Grounded Gate (Pin 11)

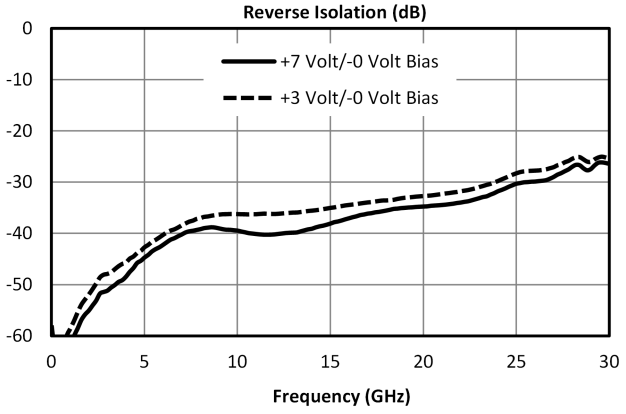
Small Signal Gain (dB)



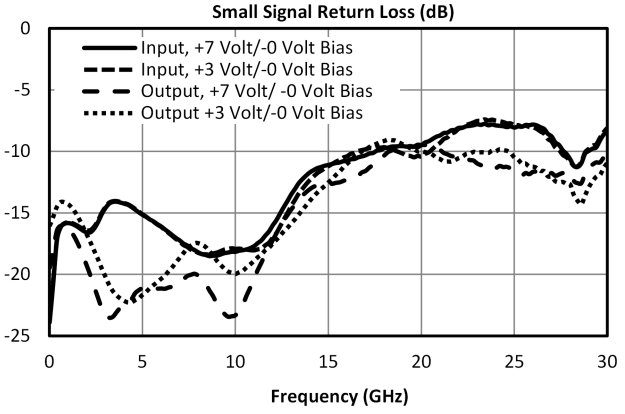
Saturated Output Power (dBm)



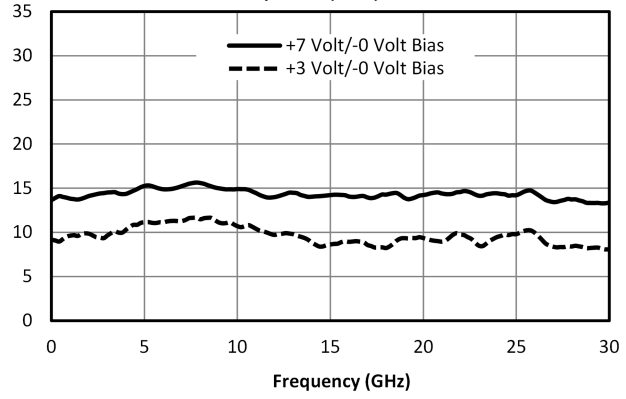
Reverse Isolation (dB)



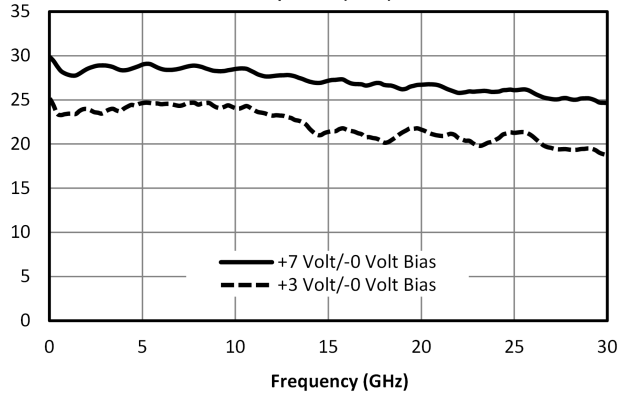
Small Signal Return Loss (dB)



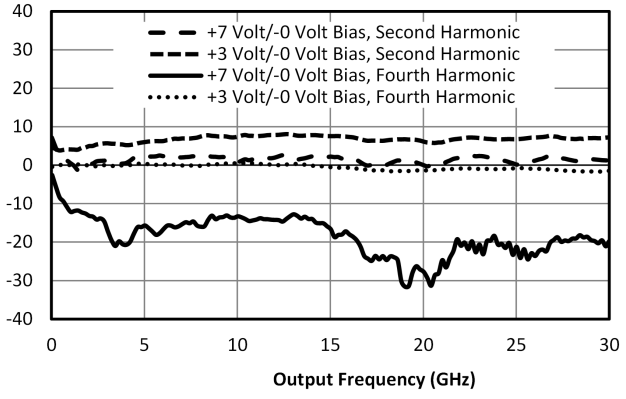
Input IP3 (dBm)



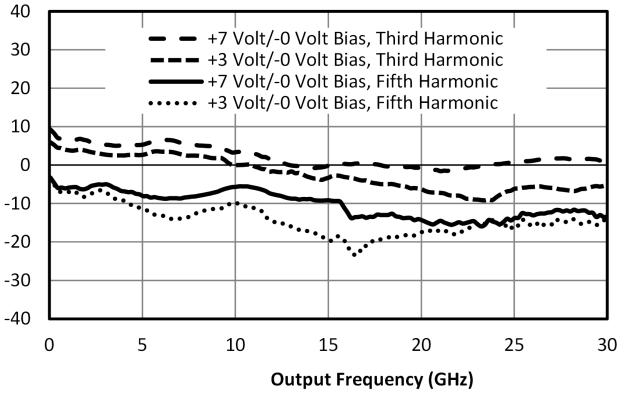
Output IP3 (dBm)

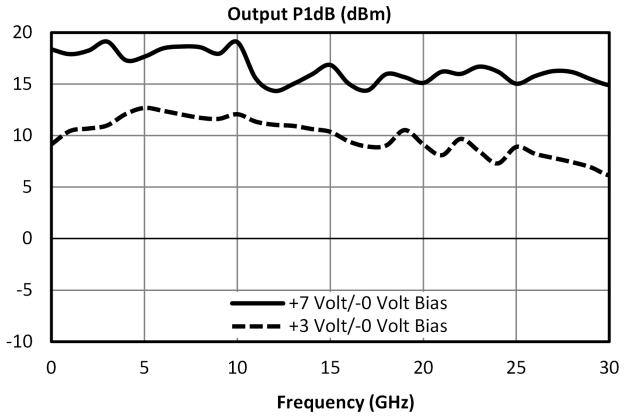


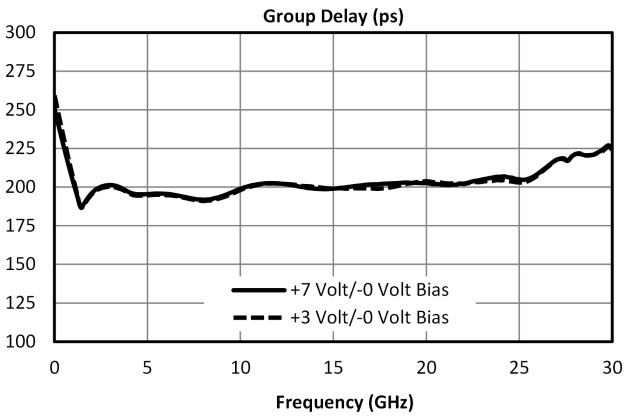
Even Harmonic Generation (dBm) +10 dBm Input

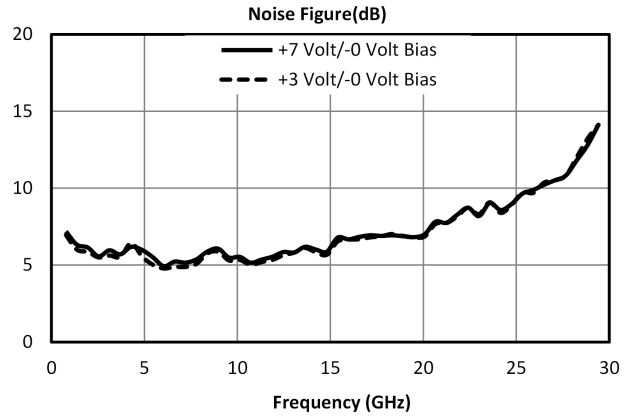


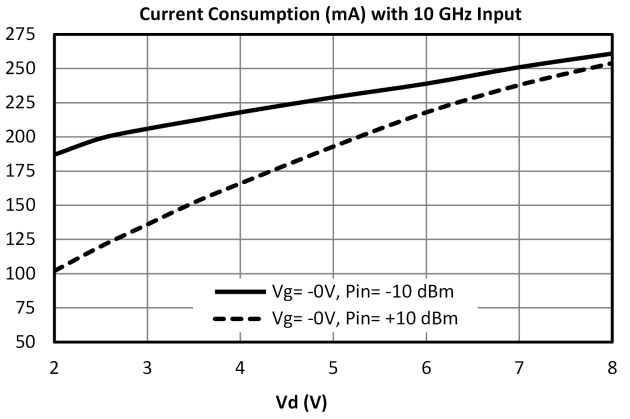
Odd Harmonic Generation (dBm) +10 dBm Input





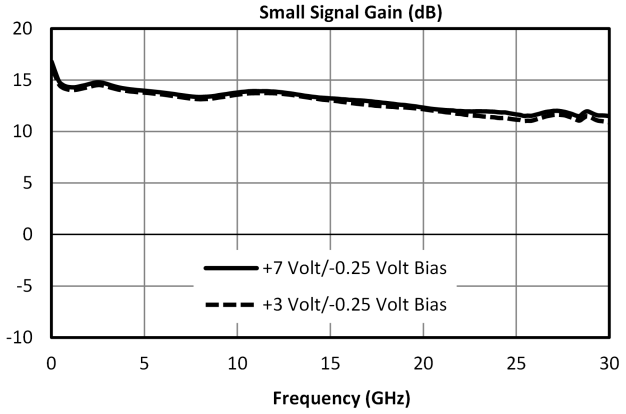




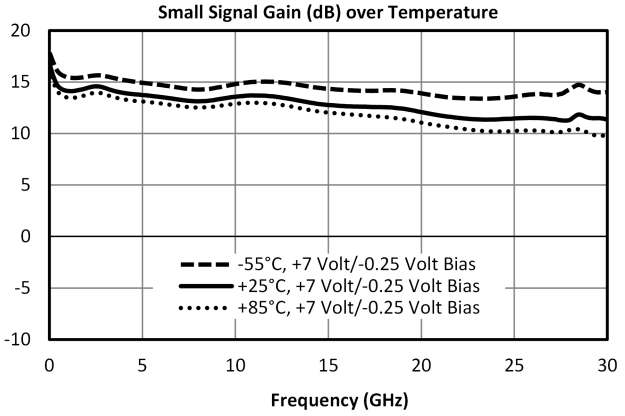


Typical Performance Plots - +5 to +7V Positive Bias (Pin 16 Output), -.25 Negative Bias (Pin11)

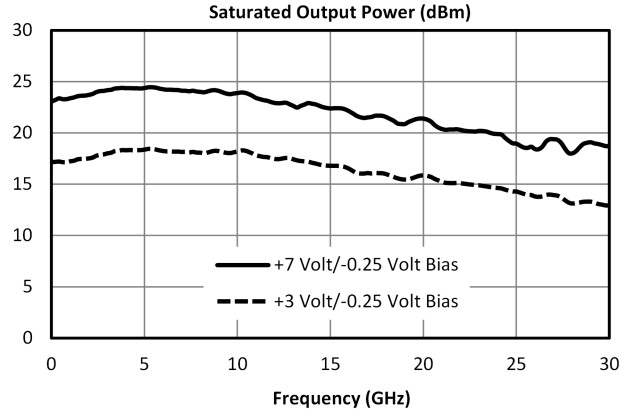
Small Signal Gain (dB)



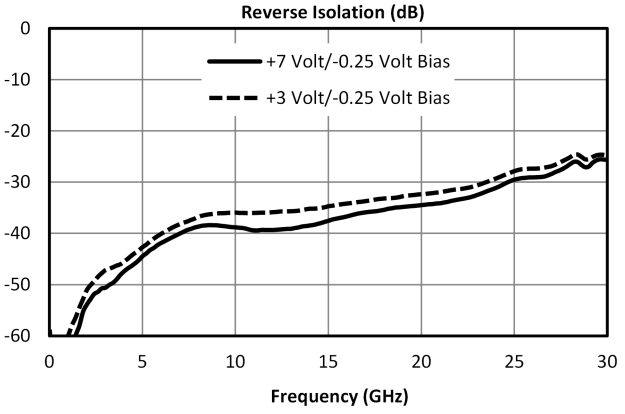
Small Signal Gain (dB) over Temperature



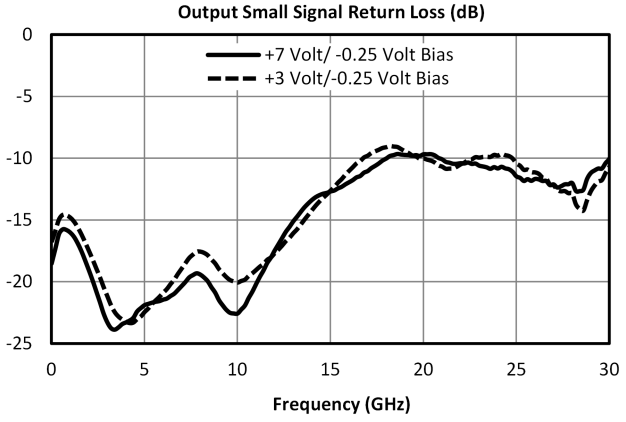
Saturated Output Power (dBm)



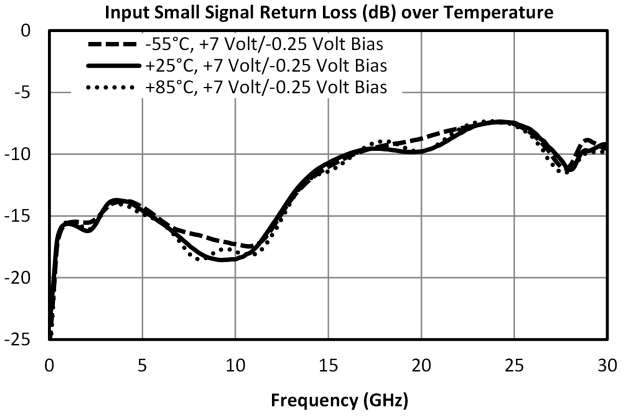
Reverse Isolation (dB)



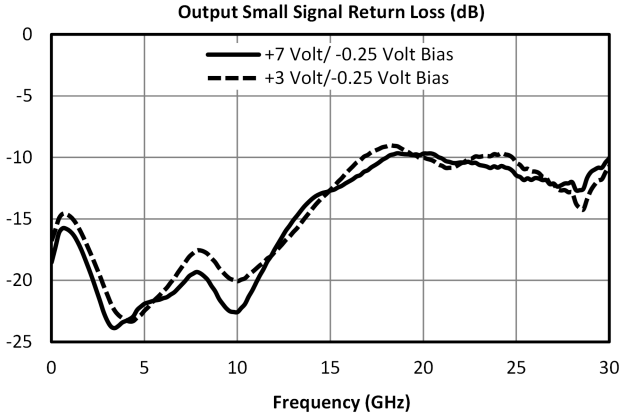
Output Small Signal Return Loss (dB)



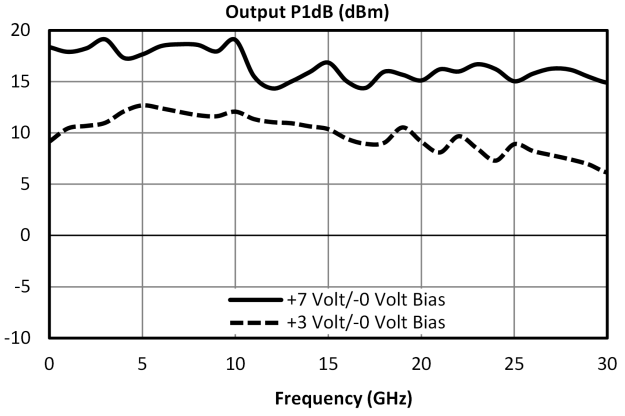
Input Small Signal Return Loss (dB) over Temperature



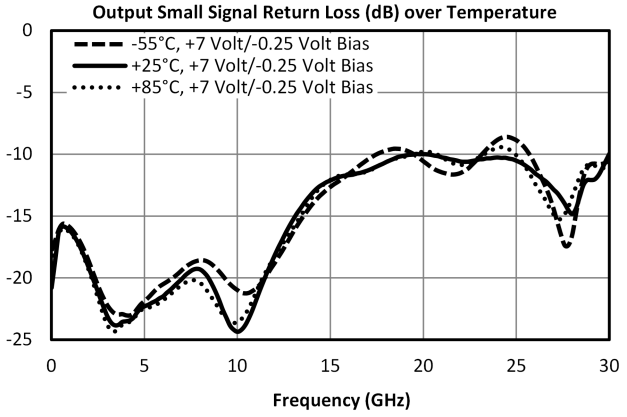
Output Small Signal Return Loss (dB)



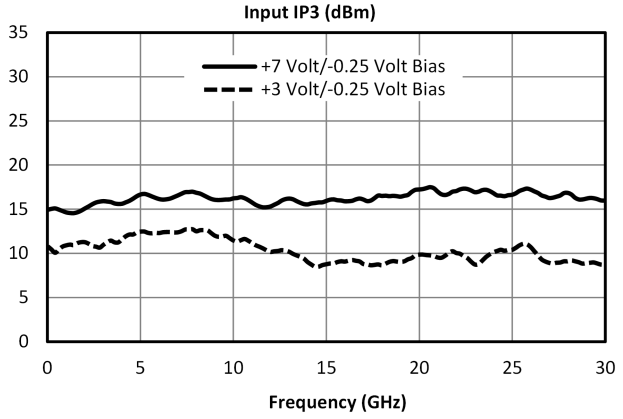
Output P1dB (dBm)



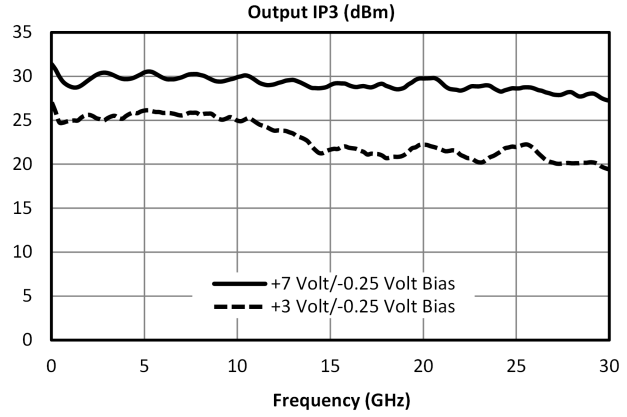
Output Small Signal Return Loss (dB) over Temperature



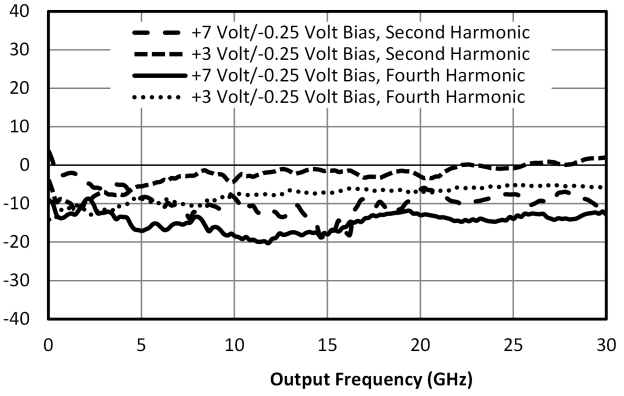
Input IP3 (dBm)



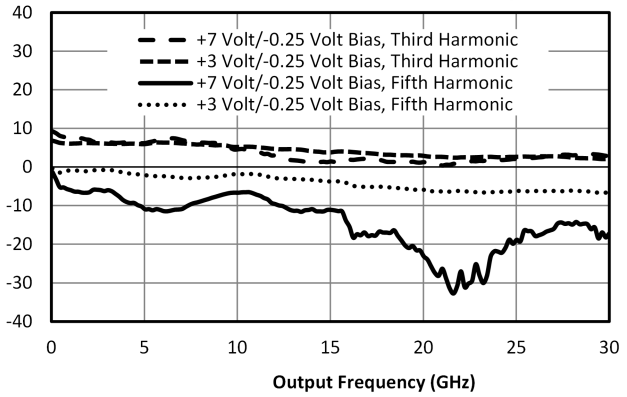
Output IP3 (dBm)



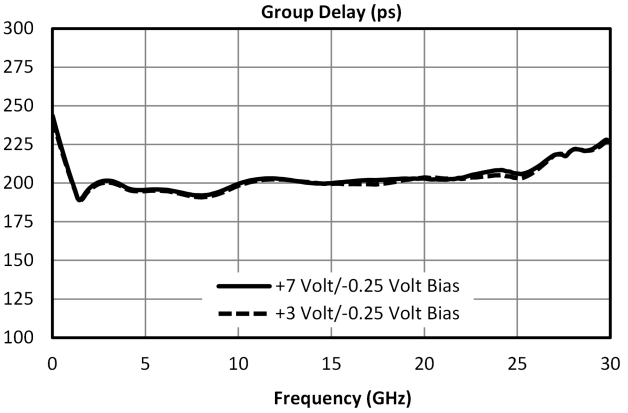
Even Harmonic Generation (dBm) +10 dBm Input



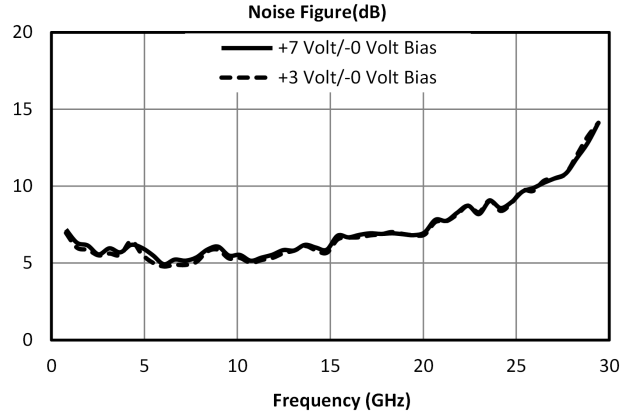
Odd Harmonic Generation (dBm) +10 dBm Input



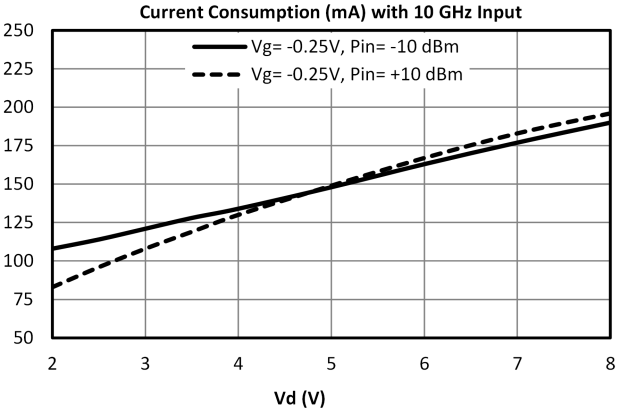
Group Delay (ps)



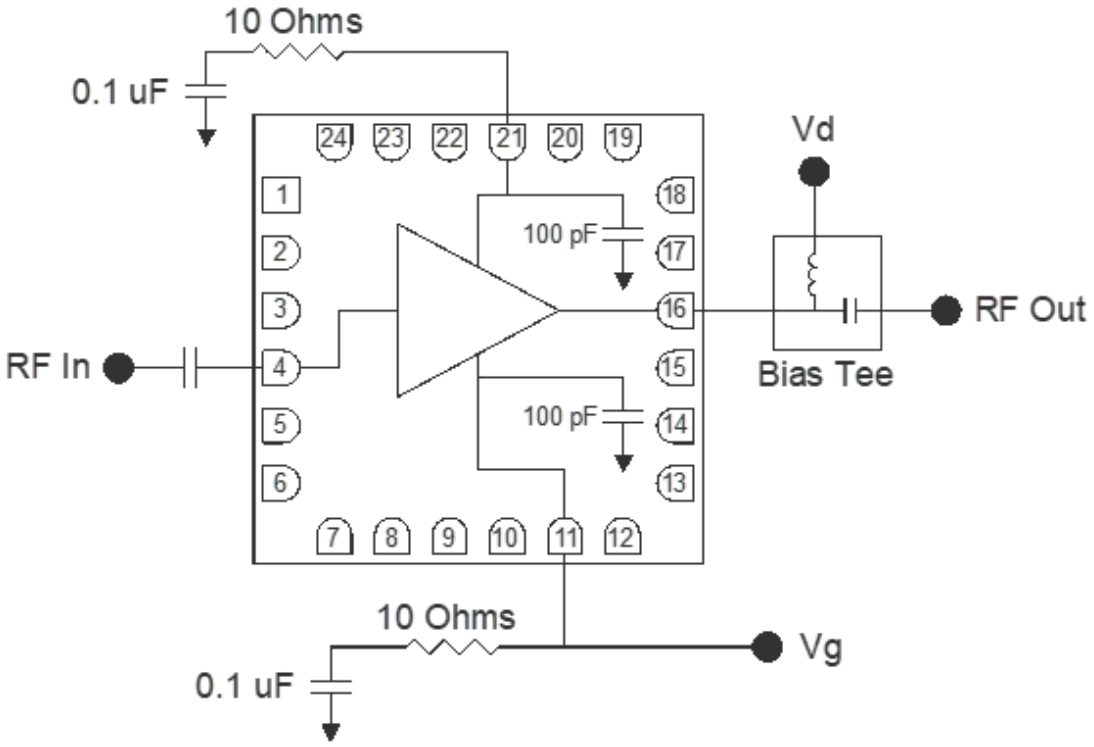
Noise Figure(dB)



Current Consumption (mA) with 10 GHz Input



Application Circuit



Application Circuit Description

Biasing and Operation

RF In / RF Out – Input and output signals should be connected by 50 ohm microstrip or coplanar traces to well matched 50 ohm sources and loads. DC blocking capacitors and bias tees are required.

Vg – Negative gate voltage is optional, the amplifier can operate with positive bias only. Application of a negative bias between 0 and -0.3V will reduce current consumption, improve even harmonic suppression, and potentially improve T3 linearity. Reduced current consumption can also lead to increased amplifier lifetime. The amplifier is designed for optimal performance when the negative gate voltage is tuned such that current drawn from the positive bias supply is 165 mA. It may be supplied through pin 11 or through the RF input on pin 4.

Vd- Bias supply supplied to Vd through pin 16 should be voltage limited below 9 V and current limited below 275 mA at all times. The operational bias voltage should be between 5 V and 7 V for full gain, efficiency, and linearity. In general gain, linearity, and output power will increase marginally with increased voltage from 5 to 7 V.

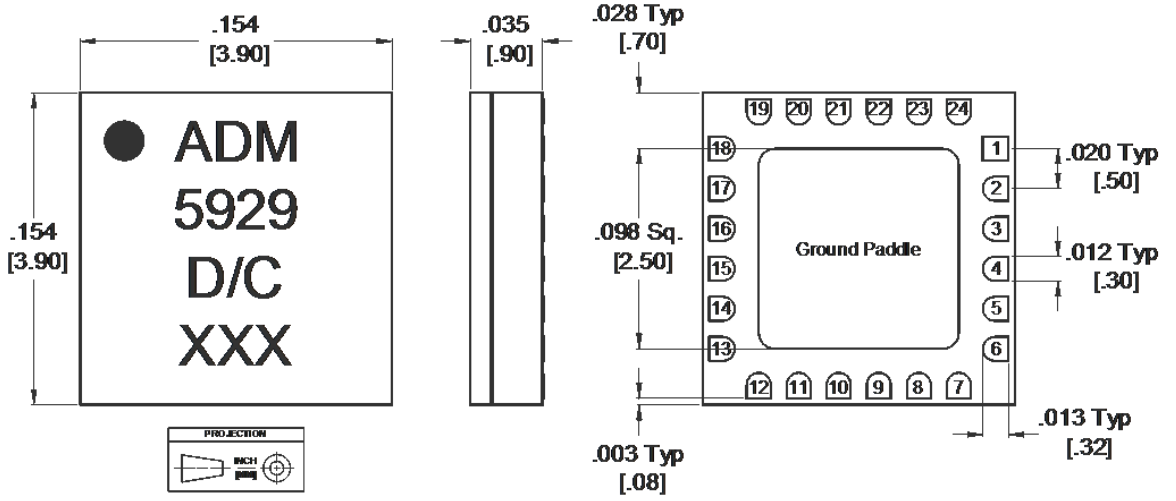
Optional Bias Circuitry – The resistor and capacitor on the Vd and Vg lines (pads 21 and 11) prevent low frequency oscillation. These components are not required in bias circuits with sufficient low frequency loss. Designers should experiment to determine if they are necessary.

DC/RF Ground – The ground paddle of the QFN should be connected to a low noise RF and DC ground with very low electrical and thermal resistance for high frequency operation and thermal heat sinking.

Mechanical Data

Outline Drawing

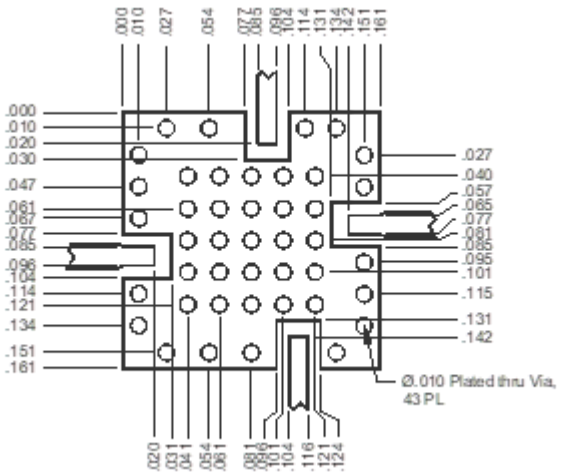
Download : Outline 2D Drawing | Outline 3D Drawing | Outline 3D STP



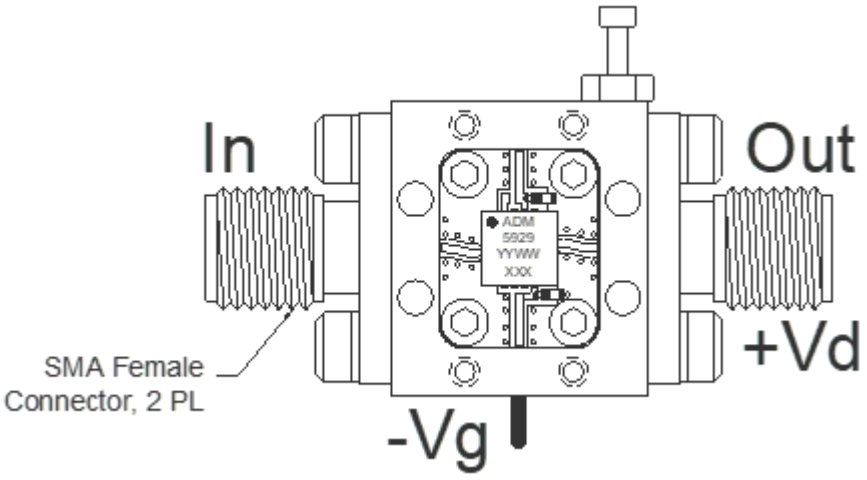
Pad #	Function
1	N/C
2	N/C
3	N/C
4	RF In
5	N/C
6	N/C
7	N/C
8	N/C
9	N/C
10	N/C
11	Vg
12	N/C
13	N/C
14	N/C
15	N/C
16	RF Out/Vd
17	N/C
18	N/C
19	N/C
20	N/C
21	Vd2
22	N/C
23	N/C
24	N/C

Footprint Image

Download : Footprint Drawing



Evaluation Board - Outline Drawing



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