Sales: 408-778-9952 | General: 408-778-4200 | Fax: 408-778-4300
Sales & Customer Support: sales@markimicrowave.com
Tech Support: support@markimicrowave.com

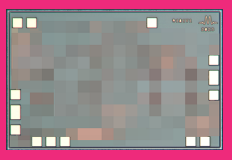
ADM-9181CH

DC - 26 GHz Distributed Amplifier

DEVICE OVERVIEW

General Description

The ADM-9181CH is a wideband distributed amplifier capable of providing 14.5 dB gain and +31 dBm OIP3 from 100MHz to 22 GHz. The ADM-9181CH is an ideal linear signal amplifier for applications requiring low power consumption and small form-factors. The amplifier has excellent return losses and gain flatness.



Download s-parameters here

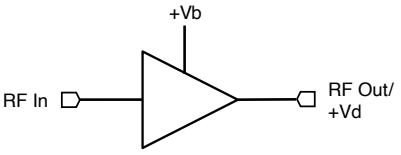
Features

- 14.5dB typical gain Gain
- +31dBm typical OIP3
- Flat gain response
- Excellent return losses

Applications

- Communication Systems
- Test and Measurement Equipment
- Satellite Communications
- Electronic Warfare

Functional Block Diagram



Part Ordering Options

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
ADM-9181CH	DC - 26 GHz Distributed Amplifier	CH	RoHS	Released	EAR99

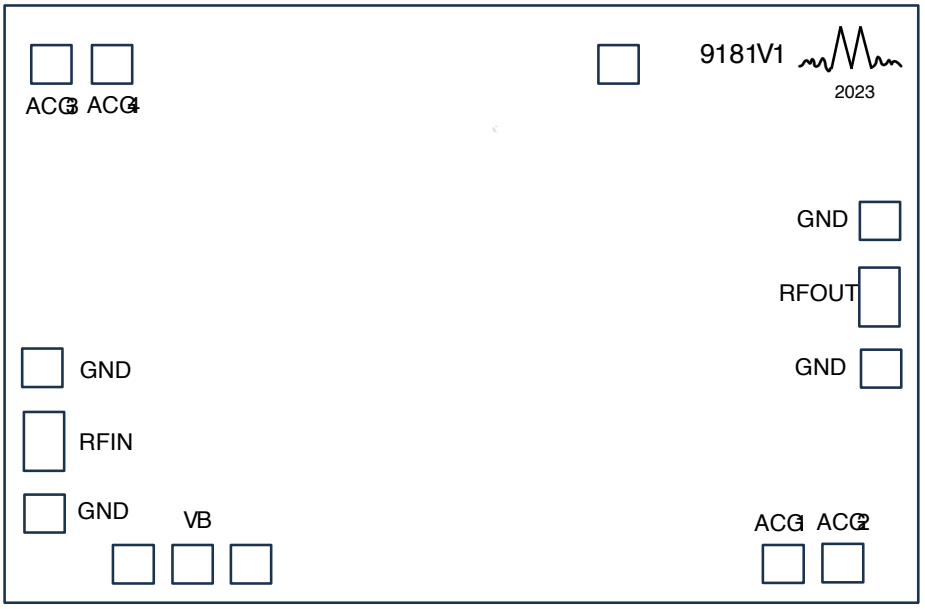
Table Of Contents

Revision History

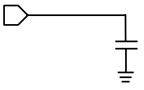
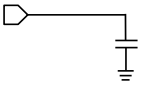
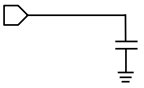
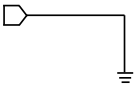
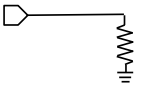
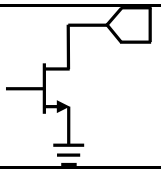
Revision Code	Revision Date	Comment
-	2024-08-29	Initial Release

Port Configuration and Functions

Port Diagram



Port Functions

Port	Function	Description	Equivalent Circuit for Package
ACG1	External Chip Capacitor	The ACG1 pad provides additional off chip bypass capacitance. A 0.1uF chip capacitor is recommended.	
ACG2	External Chip Capacitor	The ACG2 pad provides additional off chip bypass capacitance. A 100pF chip capacitor is recommended.	
ACG3	External Chip Capacitor	The ACG3 pad provides additional off chip bypass capacitance. A 100pF chip capacitor is recommended.	
ACG4	External Chip Capacitor	The ACG4 pad provides additional off chip bypass capacitance. A 0.1uF chip capacitor is recommended.	
GND	Gnd	Gnd is provided through the backside of the die and should be connected to a DC/RF ground potential with high thermal and electrical conductivity.	
RF In	RF Input	This is the amplifier's RF Input port. It is RF matched to 50 Ω and requires a DC blocking capacitor.	
RF Out / Vd	RF Out / Vd	The RF Out/ Vd pad supplies DC voltage to the drain of the amplifier IC and also acts as the RF output. This pad requires an external bias-tee. Nominal voltage for Vd at this pad is +6V.	
Vb	Positive bias	The Vb pad provides a required positive bias which supplies an internal current mirror. A higher voltage results in higher current draw through the VD / RF Out port. This port should be set to +3V for normal operation.	

Specifications

Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If any one of these limits are exceeded, the device may become inoperable or have a reduced lifetime. Reliability limits are individual, instantaneous catastrophic limits only. Functional operation limits are indicated below. Operation of the device at multiple absolute maximum limits or for extended periods at a single limit can cause degradation and damage to the device.

Parameter	Maximum Rating	Unit
Bias Supply Voltage (Vb)	6.5	V
Drain Current (Id) (No RF Applied)	250	mA
Maximum Operating Temperature for MTTF > 1E6 hours	85	°C
Maximum Storage Temperature	125	°C
Minimum Operating Temperature for MTTF > 1E6 hours	-40	°C
Minimum Storage Temperature	-65	°C
Positive Drain Supply Voltage (Vd)	8	V
RF Input Power	20	dBm

Package Information

Parameter	Details	Rating
Dimensions	-	2.3 x 1.5 mm

Recommended Operating Conditions

The Recommended Operating Conditions indicate the limits, inside which the device should be operated, to guarantee the performance given in Electrical Specifications Operating outside these limits may not necessarily cause damage to the device, but the performance may degrade outside the limits of the electrical specifications. For limits, above which damage may occur, see Absolute Maximum Ratings.

Parameter	Min	Nominal	Max	Unit
Positive DC Current (Id) (No RF Input)	82	130	190	mA
Ambient Temperature	-40	25	85	°C
Positive DC Bias Voltage (Vb)	2	3	4.4	V
Positive DC Voltage (Vd)	4	5	6	V

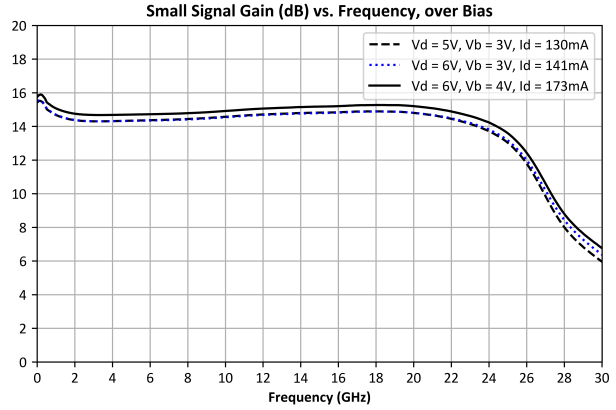
Electrical Specifications

Parameter	Test Conditions	Minimum Frequency (GHz)	Maximum Frequency (GHz)	Min	Typ	Max	Unit
Input IP2 [1]	Vd = 6V, Vb = 3V, Pin = -20dBm	0.1	13	-	24	-	dBm
Input IP3	Vd = 6V, Vb = 3V, Pin = -20dBm	0.1	26	-	17	-	dBm
Input Return Loss	Vd = 6V, Vb = 3V, Pin = -20dBm	0.1	26	-	19	-	dB
Noise Figure	Vd = 6V, Vb = 3V, Pin = -20dBm	6	26	-	3.4	-	dB
Noise Figure	Vd = 6V, Vb = 3V, Pin = -20dBm	0.1	6	-	6	-	dB
Output IP2 [2]	Vd = 6V, Vb = 3V, Pin = -20dBm	0.1	13	-	38	-	dBm
Output IP3	Vd = 6V, Vb = 3V, Pin = -20dBm	0.1	26	-	31	-	dBm
Output P1dB	Vd = 6V, Vb = 3V	0.1	20	-	22	-	dBm
Output P1dB	Vd = 6V, Vb = 3V	20	26	-	18.5	-	dBm
Output Return Loss	Vd = 6V, Vb = 3V, Pin = -20dBm	0.1	26	-	23	-	dB
Reverse Isolation	Vd = 6V, Vb = 3V, Pin = -20dBm	0.1	26	-	38	-	dB
Small Signal Gain	Vd = 6V, Vb = 3V, Pin = -20dBm	0.1	26	-	14.5	-	dB

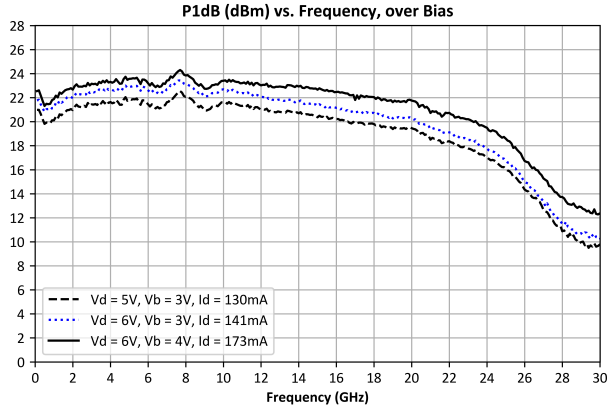
[1][2] IP2 is specified up to an input frequency of 13GHz where the IM2 product becomes attenuated by the frequency response of the amplifier.

Typical Performance vs. Bias

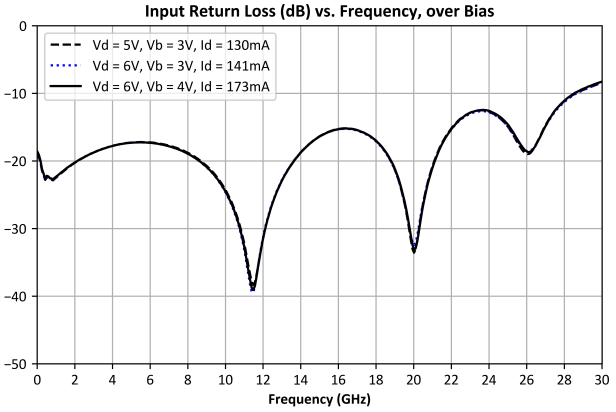
Small Signal Gain (dB) vs. Frequency, over Bias



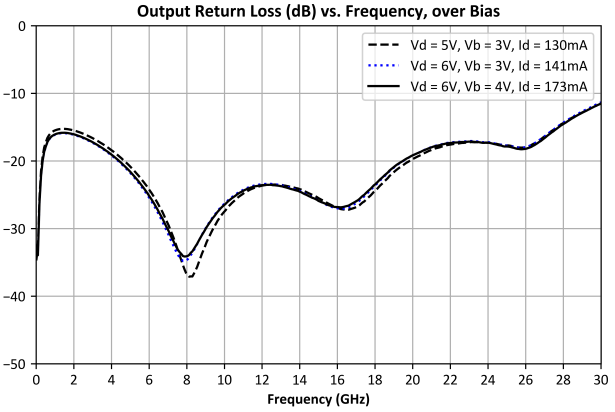
P1dB (dBm) vs. Frequency, over Bias



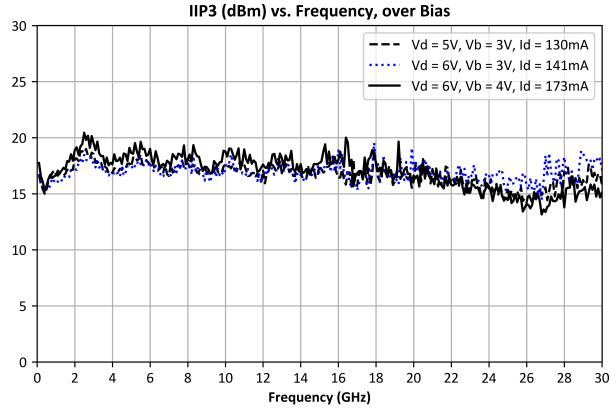
Input Return Loss (dB) vs. Frequency, over Bias



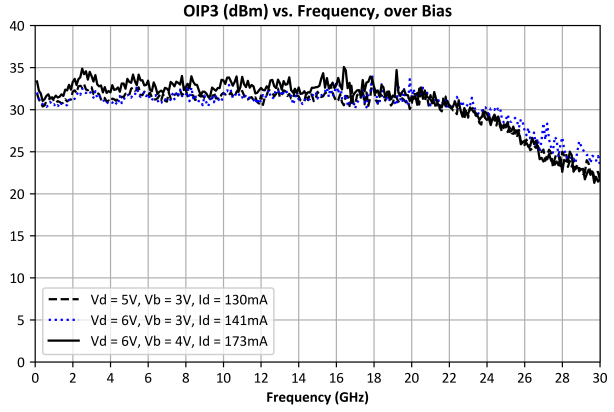
Output Return Loss (dB) vs. Frequency, over Bias



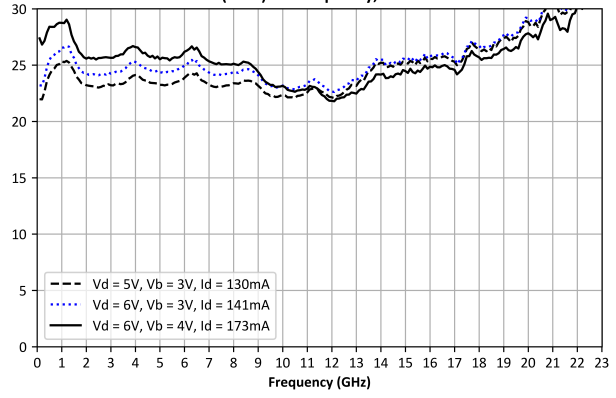
IIP3 (dBm) vs. Frequency, over Bias



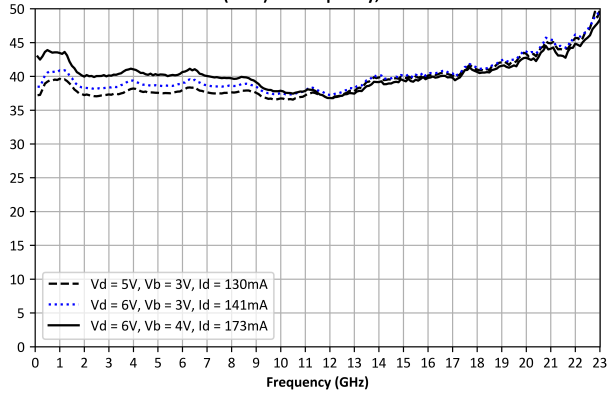
OIP3 (dBm) vs. Frequency, over Bias

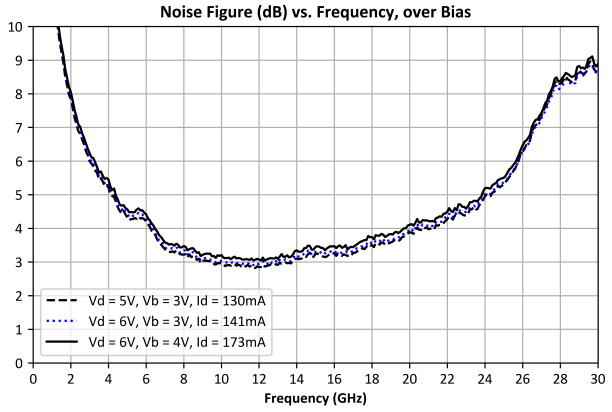


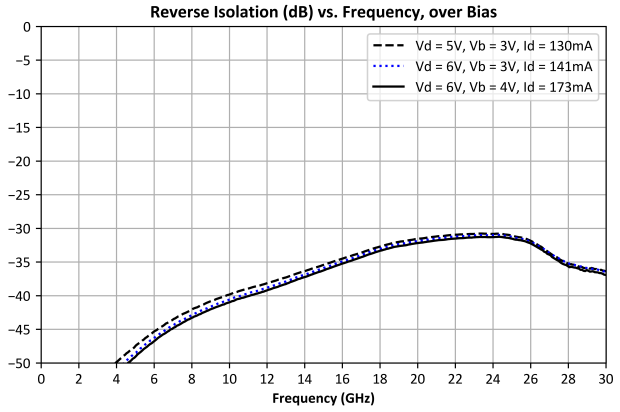
IIP2 (dBm) vs. Frequency, over Bias



OIP2 (dBm) vs. Frequency, over Bias



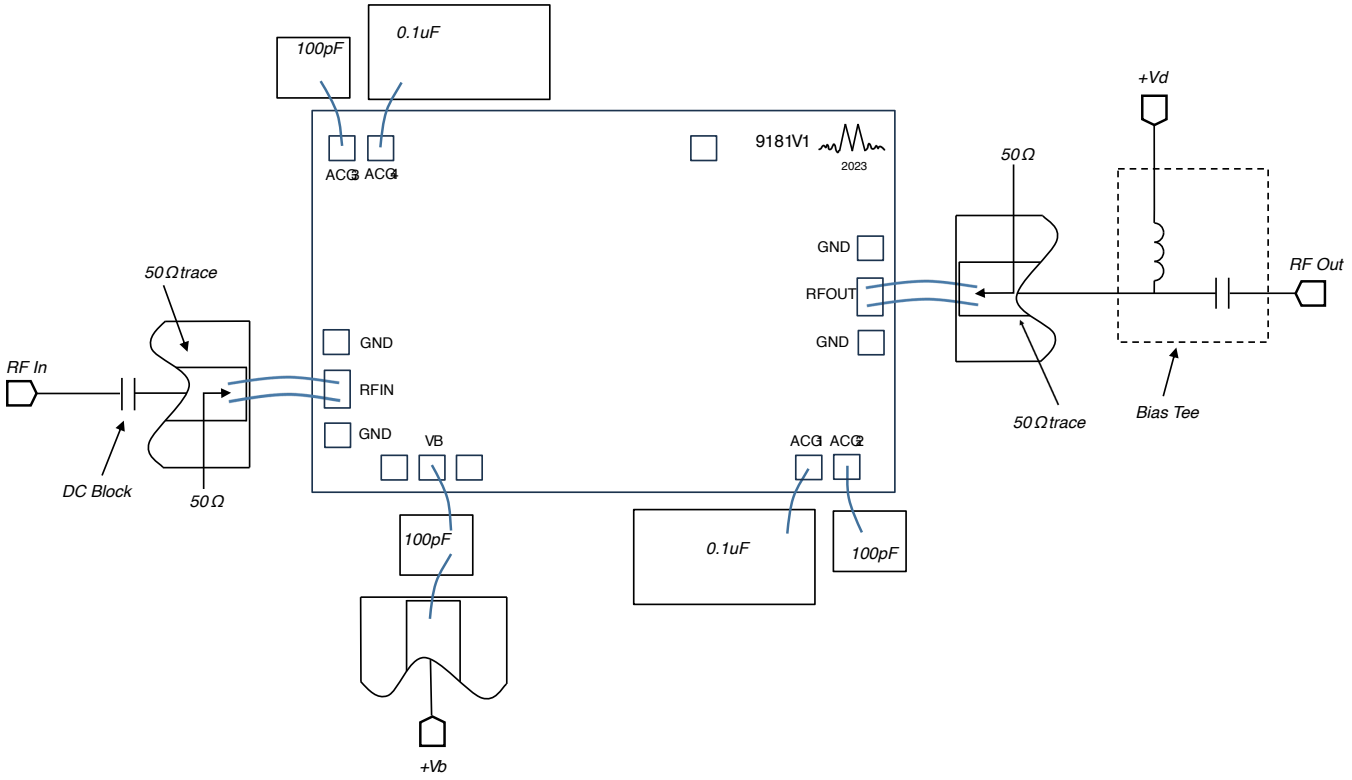




Application Information

Below is the recommended application circuit for the ADM-9181CH.

Application Circuit



Die Mounting Recommendations

Mounting and Bonding Recommendations

Marki MMICs should be attached directly to a ground plane with conductive epoxy. The ground plane electrical impedance should be as low as practically possible. This will prevent resonances and permit the best possible electrical performance. Datasheet performance is only guaranteed in an environment with a low electrical impedance ground.

Mounting - To epoxy the chip, apply a minimum amount of conductive epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip. Cure epoxy according to manufacturer instructions.

Wire Bonding - Ball or wedge bond with 0.025 mm (1 mil) diameter pure gold wire. Thermosonic wirebonding with a nominal stage temperature of 150 °C and a ball bonding force of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Use the minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should be started on the chip and terminated on the package or substrate. Bond wire inductance will improve return loss. Bondwire inductance in the range of 30pH to 200pH will improve performance.

Circuit Considerations – 50 Ω transmission lines should be used for all high frequency connections in and out of the chip. Wirebonds should be kept as short as possible, with multiple wirebonds recommended for higher frequency connections to reduce parasitic inductance. In circumstances where the chip more than .001” thinner than the substrate, a heat spreading spacer tab is optional to further reduce bondwire length and parasitic inductance.

Handling Precautions

General Handling

Chips should be handled with care using tweezers or a vacuum collet. Users should take precautions to protect chips from direct human contact that can deposit contaminants, like perspiration and skin oils on any of the chip's surfaces.

Static Sensitivity

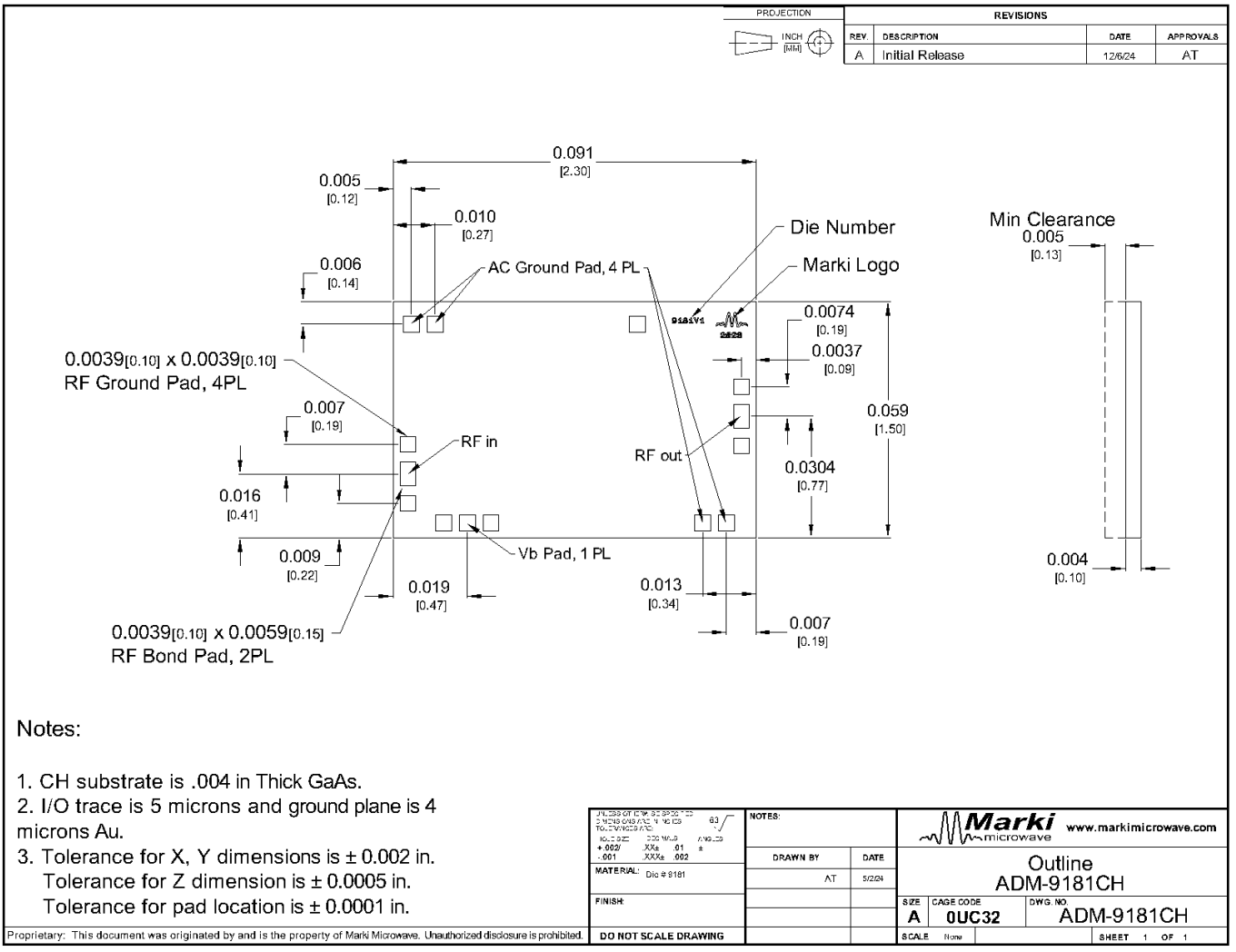
GaAs MMIC devices are sensitive to ESD and should be handled, assembled, tested, and transported only in static protected environments.

Cleaning and Storage: Do not attempt to clean the chip with a liquid cleaning system or expose the bare chips to liquid. Once the ESD sensitive bags the chips are stored in are opened, chips should be stored in a dry nitrogen atmosphere.

Mechanical Data

Outline Drawing

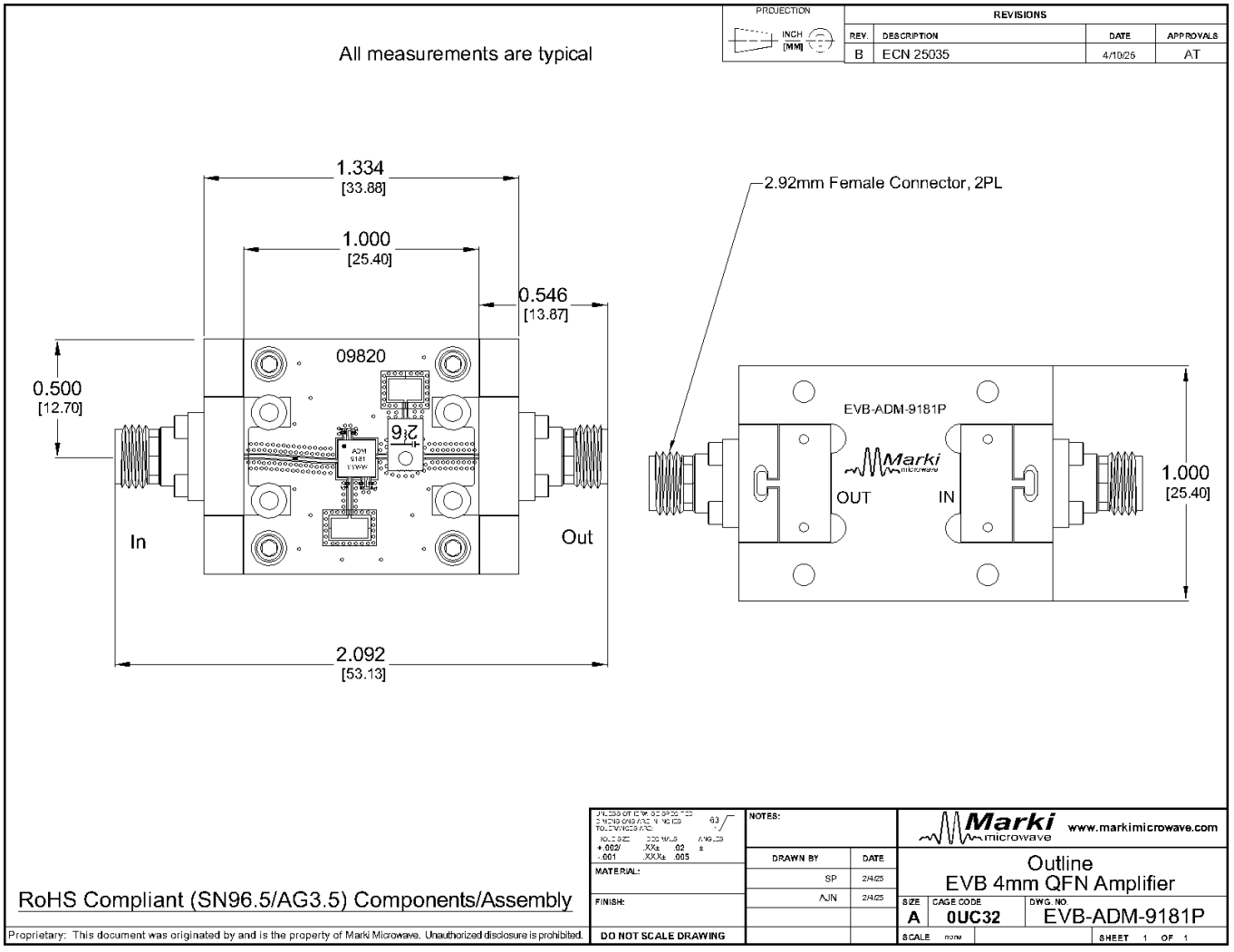
Download : Outline 2D Drawing



Notes:

1. CH substrate is 0.004 thick GaAs.
2. I/O trace is 5 microns and ground plane is 4 microns Au.
3. Tolerance for X, Y dimensions is ± 0.002 in.
4. Tolerance for Z dimensions is ± 0.0005 in.
5. Tolerance for pad location is ± 0.0001 in.

Evaluation Board - Outline Drawing



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