

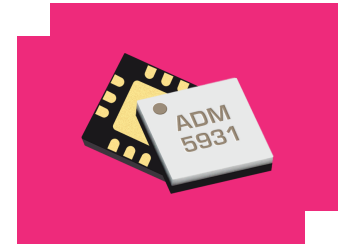
# ADM-0012-5931SM

## Broadband Distributed Amplifier

### DEVICE OVERVIEW

#### General Description

The ADM-0012-5931SM is a small, low power, and economical T3 driver or T3A pre-amplifier. It is a GaAs PHEMT distributed amplifier in a 3mm QFN surface mount package. The ADM-0012-5931SM can provide LO drive for 'L', 'M', 'I', and 'H' level mixers, with 11.5 dB typical gain and +19 dBm typical saturated output power for only 85 mA of current. The amplifier can be biased with internal circuitry, or with an external bias network for lower voltage and single supply operation.



[Download s-parameters here](#)

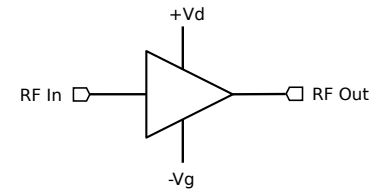
#### Features

- Optimized for use as a T3 LO buffer amplifier
- 3rd and 5th Harmonic Generation
- Suitable for driving L, M, and I diode mixers
- Optional Positive Only Bias or Internal Bias Operation
- Broadband 50 Ω Matching
- Unconditionally Stable

#### Applications

- Electronic warfare equipment
- Test and Measurement Equipment
- Amplification Clock Signals

#### Functional Block Diagram



#### Part Ordering Options

Part Number	Description	Package	Packing Size	Green Status	Product Lifecycle	Export Classification
ADM-0012-5931SM	Broadband Distributed Amplifier	QFN	-	REACH RoHS	Released	EAR99
<a href="#">EVAL3-ADM-5931</a>	Evaluation Board, Broadband Distributed Amplifier	EVAL	-	REACH RoHS	Released	EAR99
<a href="#">ADM-0012-5931TR</a>	Tape and Reel, Broadband Distributed Amplifier	QFN	7"	REACH RoHS	Released	EAR99

## Table Of Contents

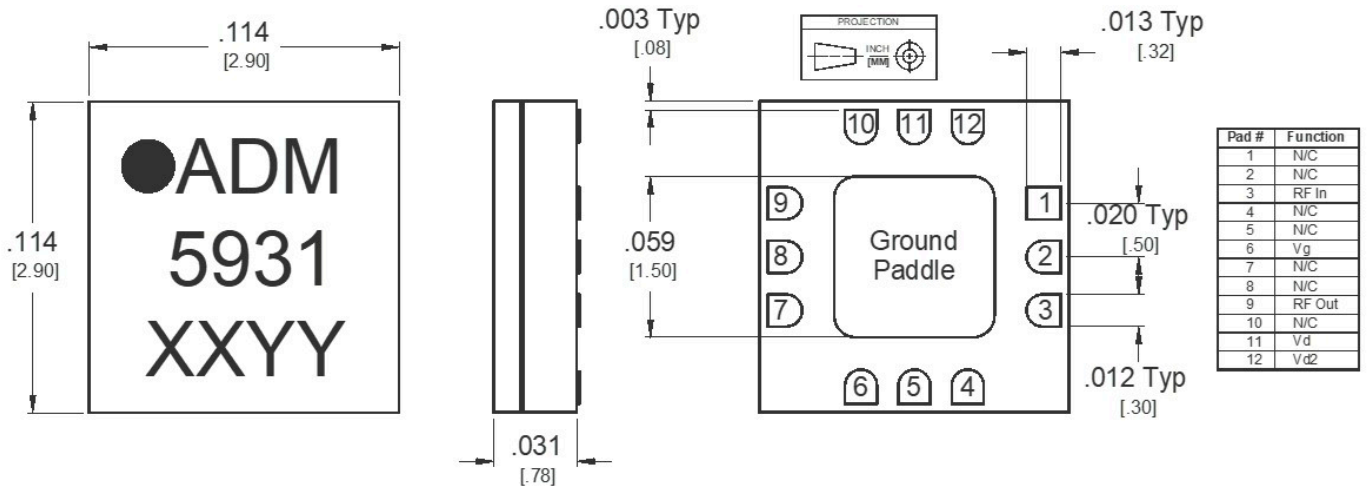
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## Revision History

Revision Code	Revision Date	Comment
-	2015-01-01	Datasheet Initial Release
A	2019-07-01	Changed thermal resistance to TBD
B	2020-12-01	Added Max Junction Temp Specification

**Port Configuration and Functions**

**Port Diagram**


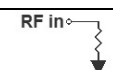
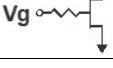

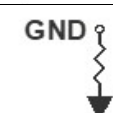


Substrate material is Ceramic.

I/O Leads and Ground Paddle are 1.4±0.6 microns (55±24 micro-inches) Au over 1.3 microns (51 micro-inches) Ni.

All unconnected pads should be connected to PCB RF ground.

**Port Functions**

Port	Function	Description	DC Equivalent Circuit
11	Vd	Power supply voltage for the amplifier. External decoupling resistor/capacitor is required.	
12	Vd2	This pin is left open for Internal Vd Bias. This pin is connected to Pin 11 (Vd) for external bias (pin 16 with bias tee).	-
1, 2, 4, 5, 7, 8, 10	NC	These pins are not connected internally. Datasheet performance is tested with NC pins grounded.	-
3	RF Input	This pin is DC coupled and matched to 50 Ω.	
6	Vg	Gate control for the amplifier. External decoupling resistor/capacitor is required.	
9	RF Output	This pad is DC coupled and matched to 50 Ω.	
Paddle	Gnd	Ground pad should be connected to RF/DC ground with low electrical and thermal resistance.	

## Specifications

### Absolute Maximum Ratings

Parameter	Maximum Rating	Unit
Maximum Operating Temperature	85	°C
Maximum Storage Temperature	150	°C
Max Junction Temperature to Maintain 10 <sup>6</sup> Hours Mean Time to Failure (MTTF):	175	°C
Minimum Operating Temperature	-55	°C
Minimum Storage Temperature	-65	°C
Negative Bias Current	2	mA
Negative Bias Voltage	-2	V
Positive Bias Voltage – Internal Bias Tee	13	V
Positive Bias Current	150	mA
Positive Bias Voltage – External Bias Tee	9	V
Power Dissipation	875	mW
RF Input Power	15	dBm

### Package Information

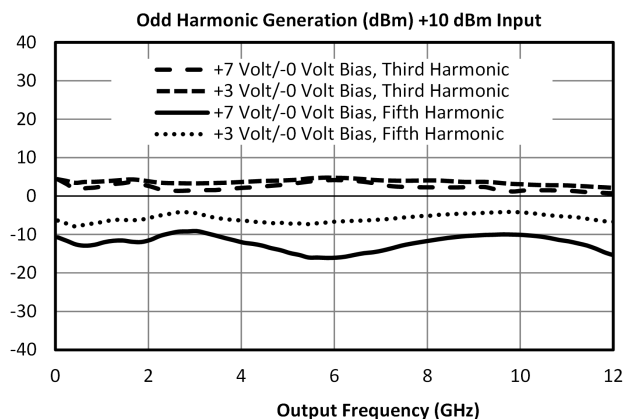
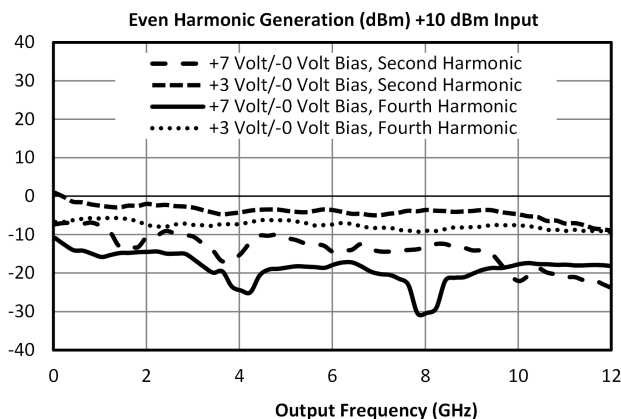
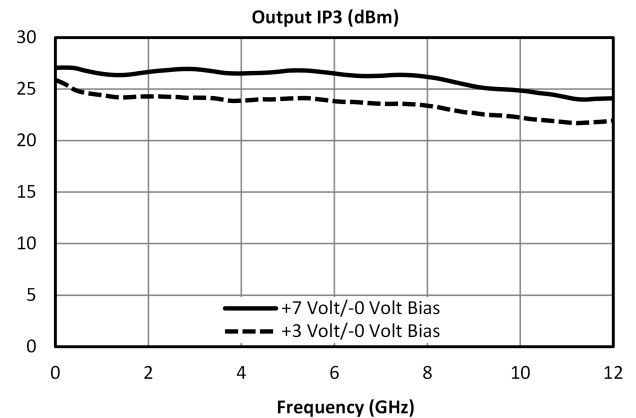
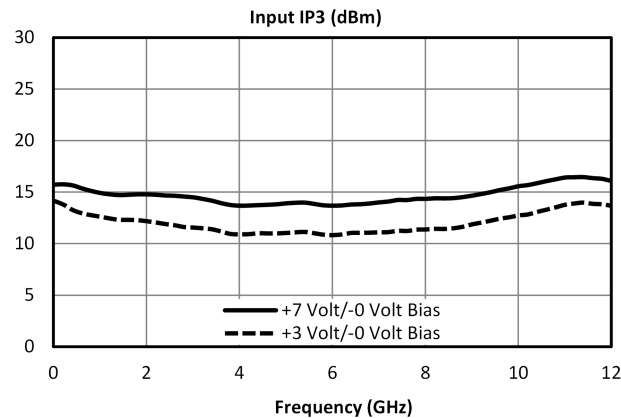
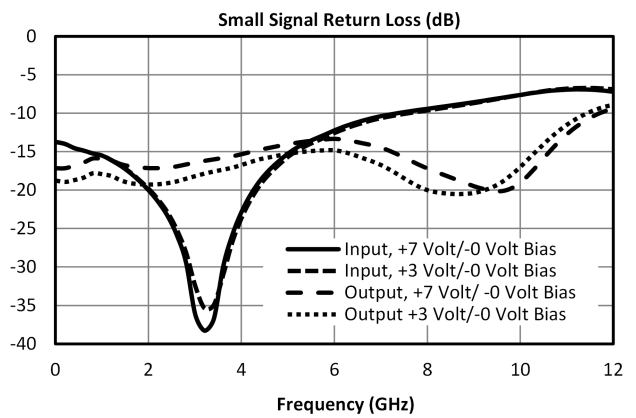
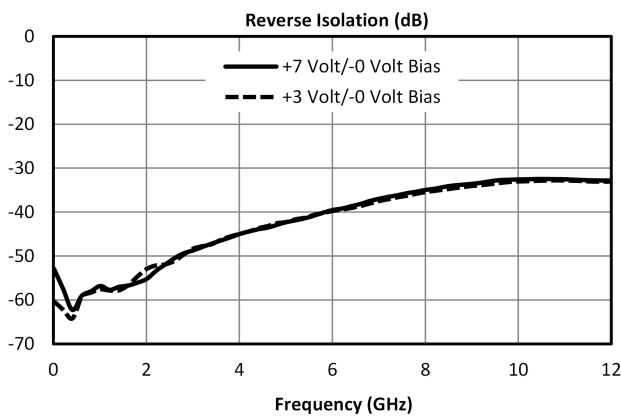
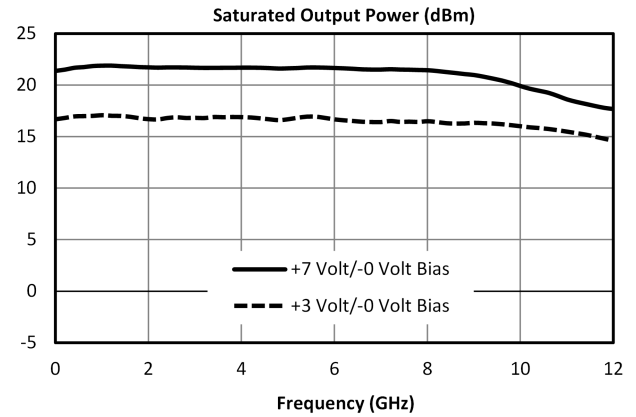
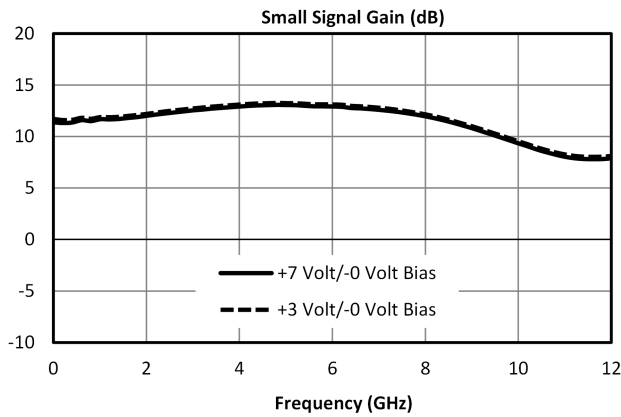
Parameter	Details	Rating
ESD	< 250 Volts	HBM Class 0
Dimensions	-	3 x 3 mm
Moisture Sensitivity Level	-	MSL 1

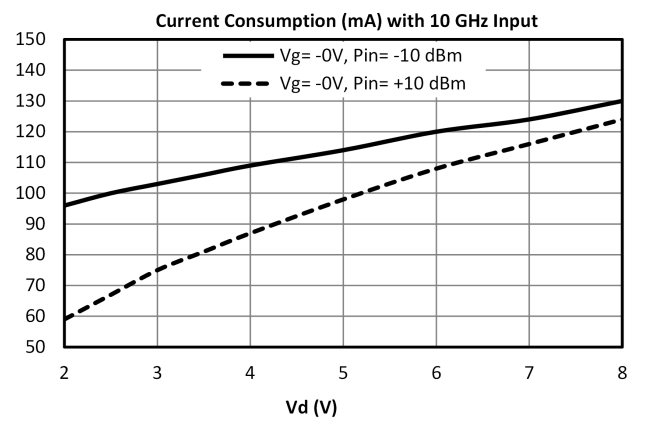
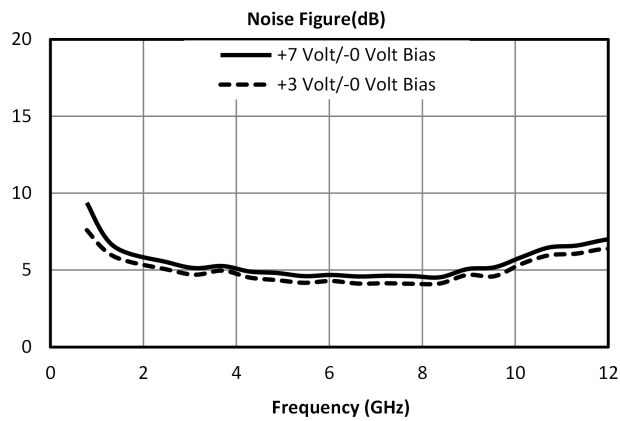
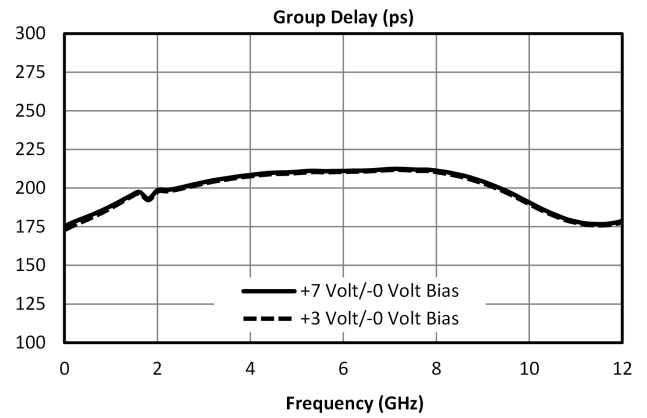
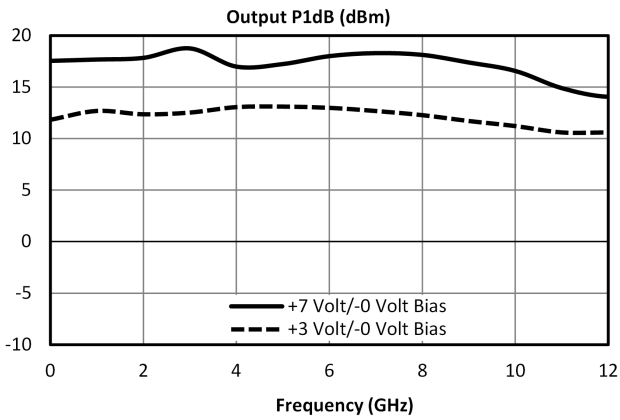
**Electrical Specifications**

Specifications measured in a 50-Ohm system.

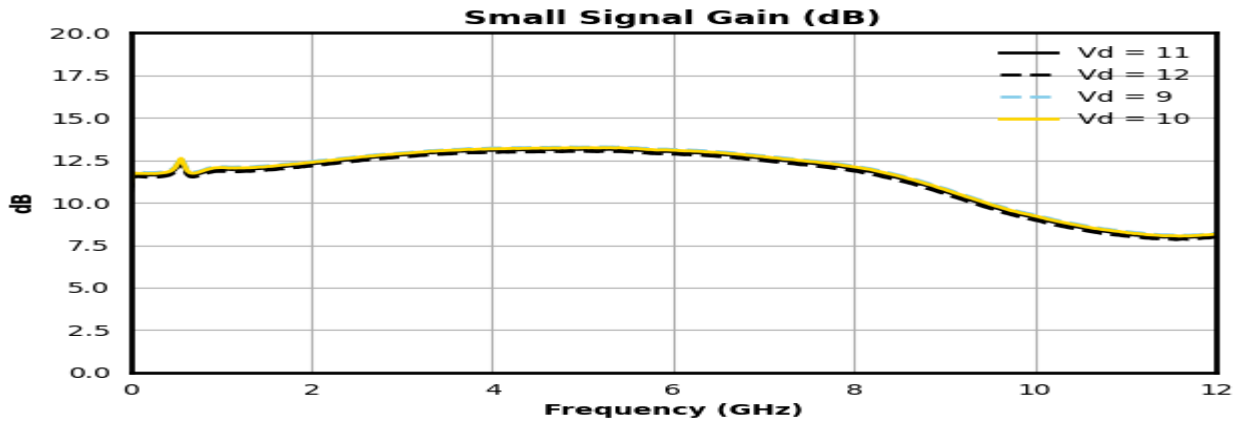
Parameter	Test Conditions	Minimum Frequency (GHz)	Maximum Frequency (GHz)	Min	Typ	Max	Unit
Bias Requirements, External	Vd: +5.0 to +7.0 Vg: -0.25 Volts	0	12	-	85	-	mA
Bias Requirements, External	Vd: +5.0 to +7.0 Vg: 0 Volts	0	12	-	115	-	mA
Bias Requirements, Internal	Vd: +10.0 to +12.0 Vg: -0.25 Volts	0	12	-	85	-	mA
Input for Saturated Output	-	0	12	5	10	12	dBm
Input Return Loss	-	0	12	-	13	-	dB
Noise Figure	-	0	12	-	4.5	-	dB
Output IP3	-	0	12	-	26	-	dBm
Output P1dB	-	0	12	-	16	-	dBm
Output Power	With Negative Bias	0	12	-	19	-	dBm
Output Return Loss	-	0	12	-	14	-	dB
Small Signal Gain	With Negative Bias	0	12	-	11.5	-	dB

**Typical Performance Plots – Positive Only (+3 to +7V) External Bias (Pin 9 Output), Grounded Gate (Pin 6)**

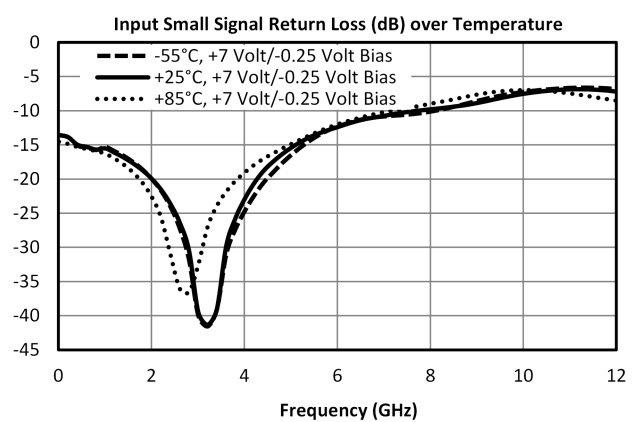
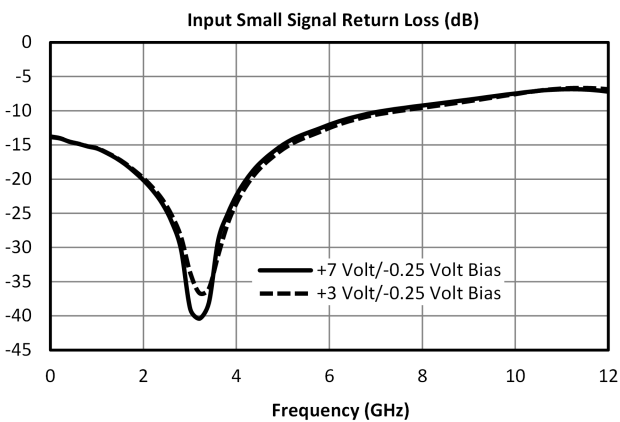
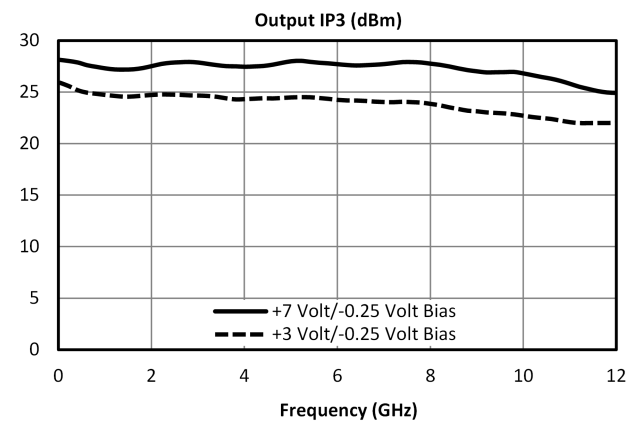
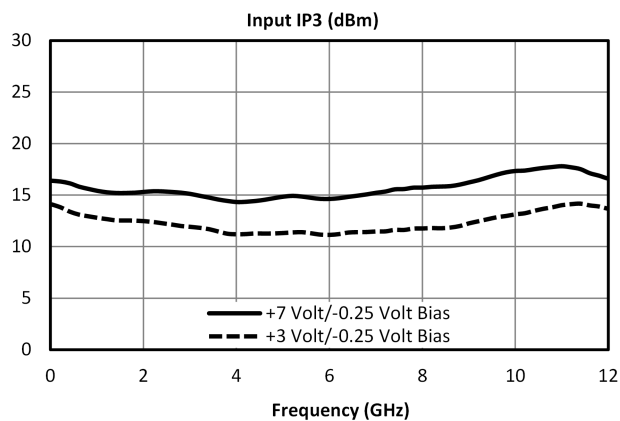
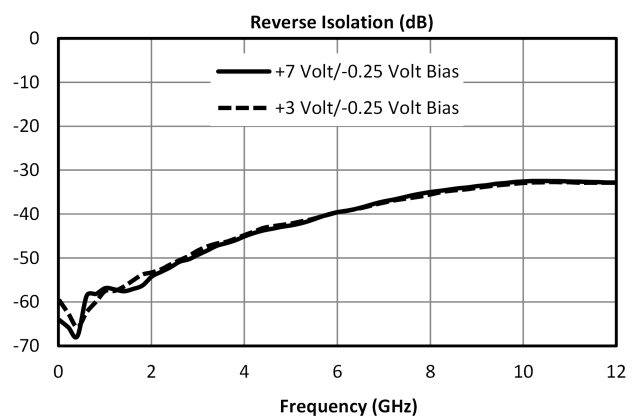
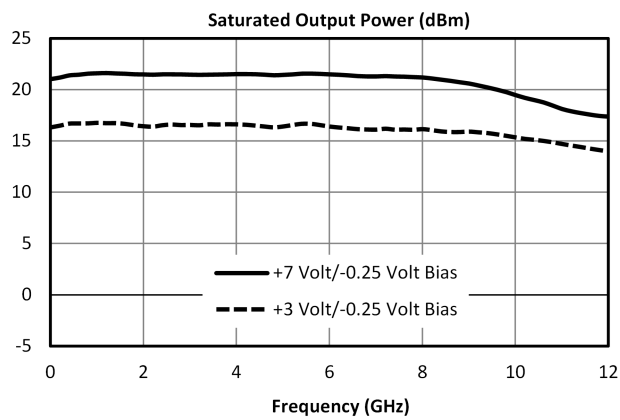
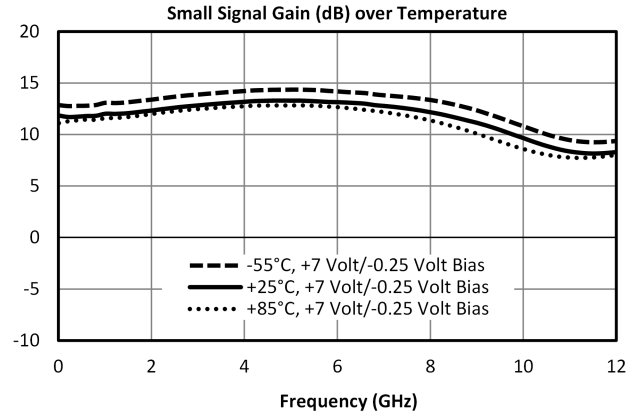
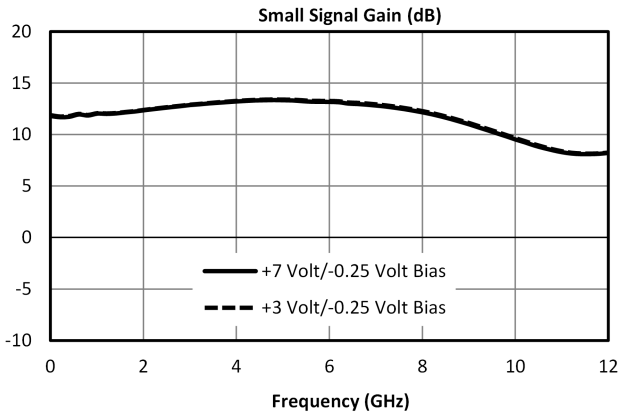


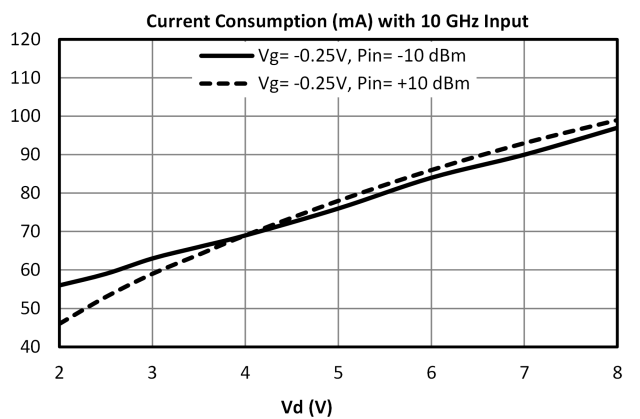
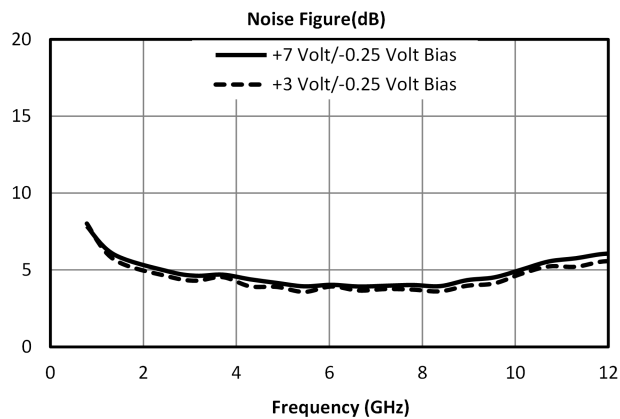
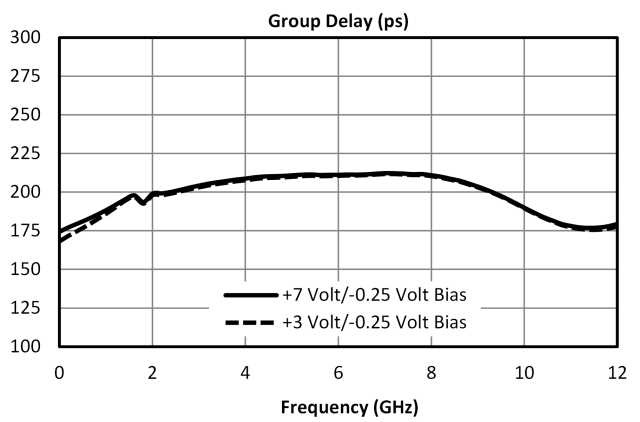
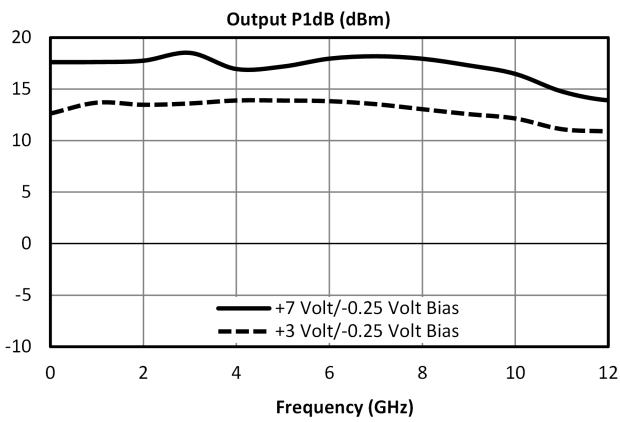
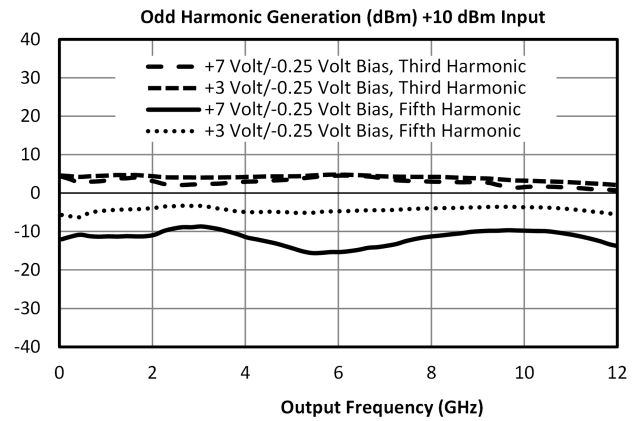
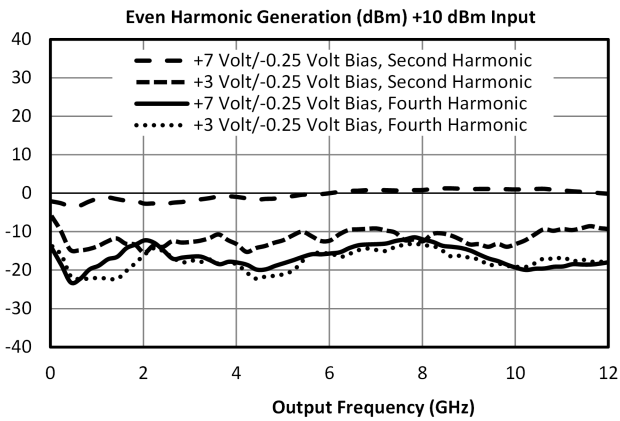
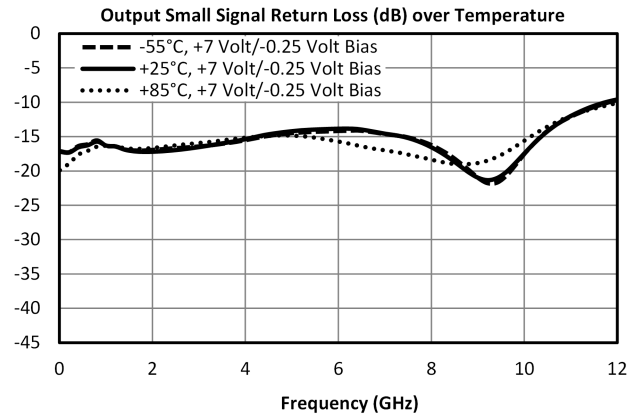
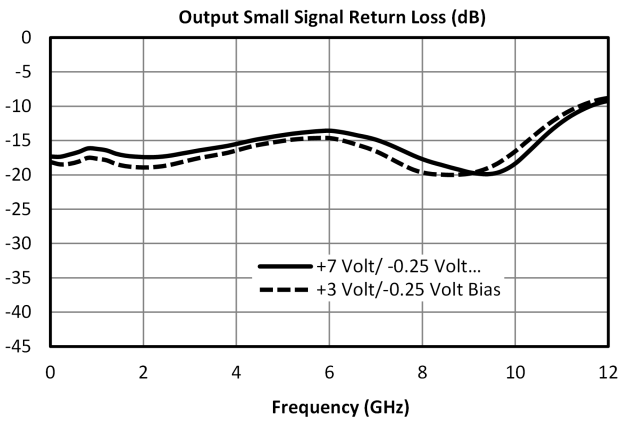


**Generated Performance Plot**

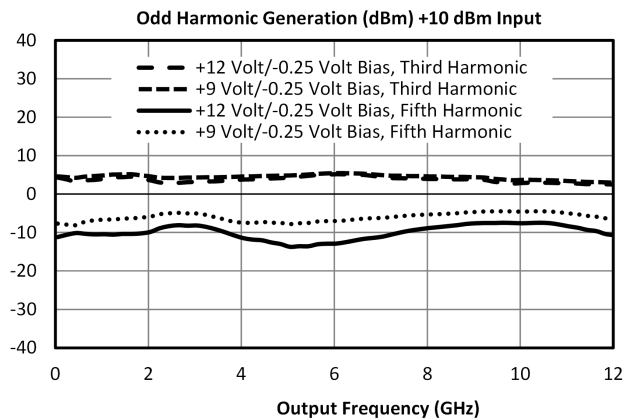
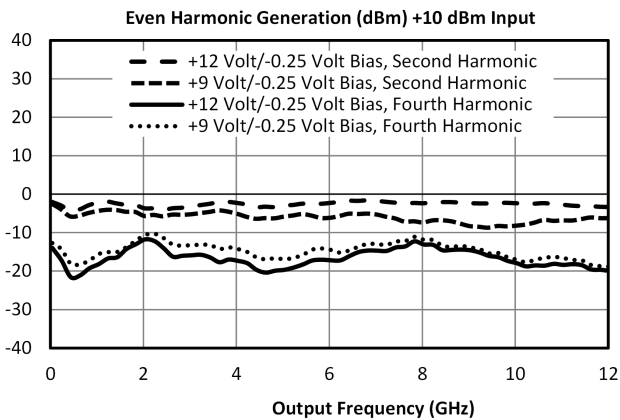
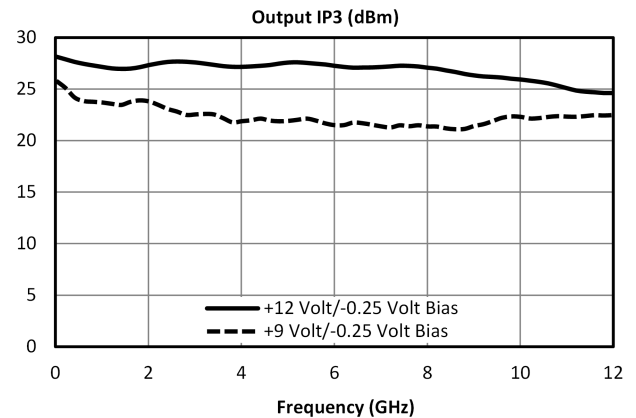
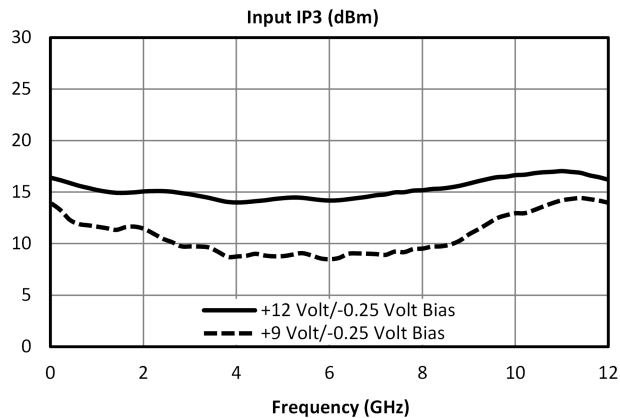
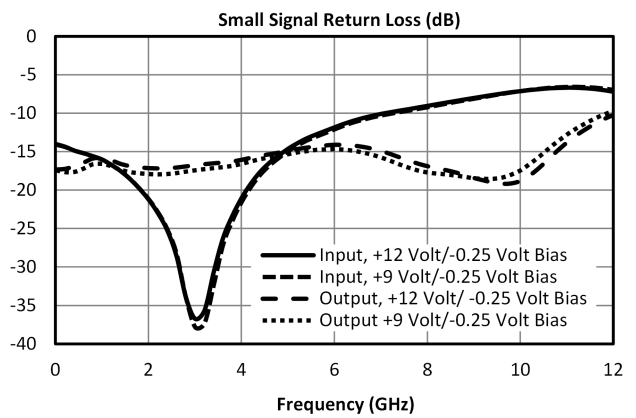
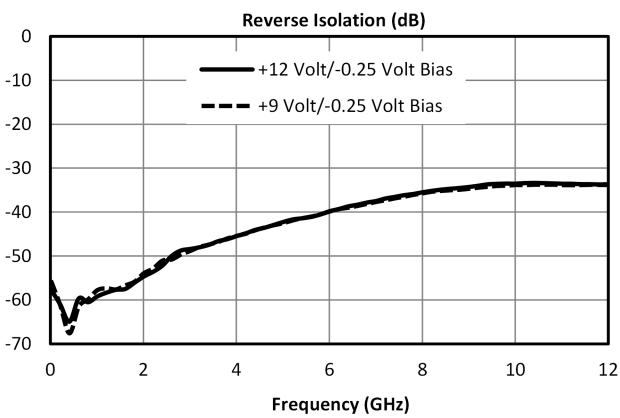
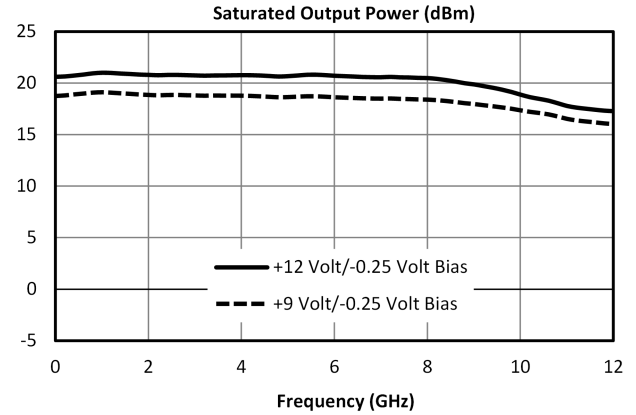
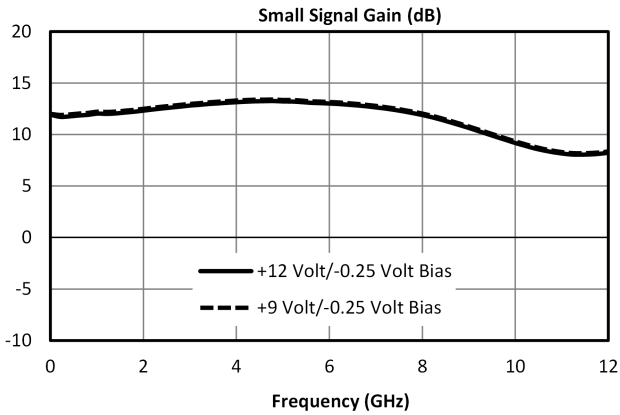


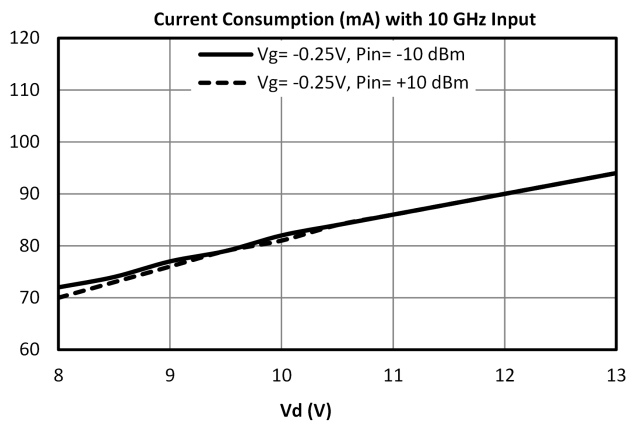
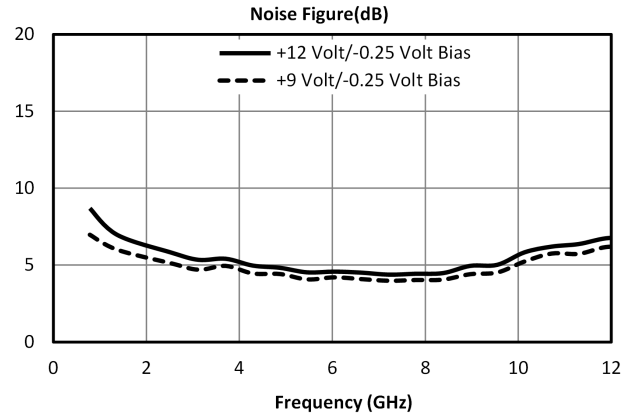
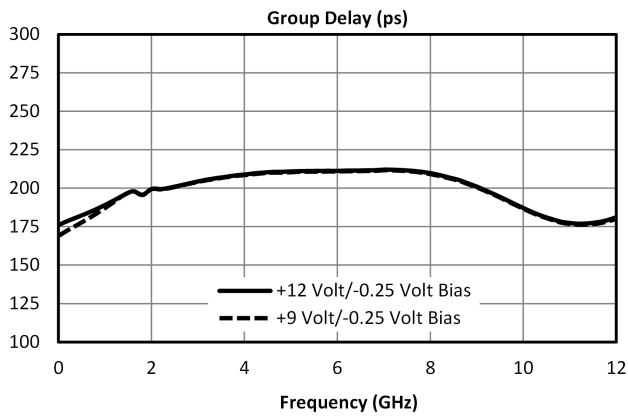
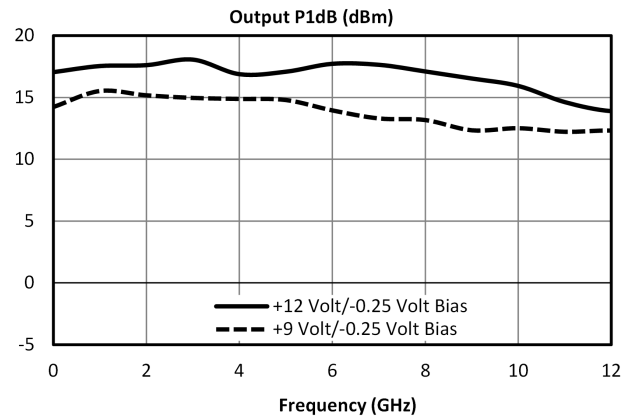
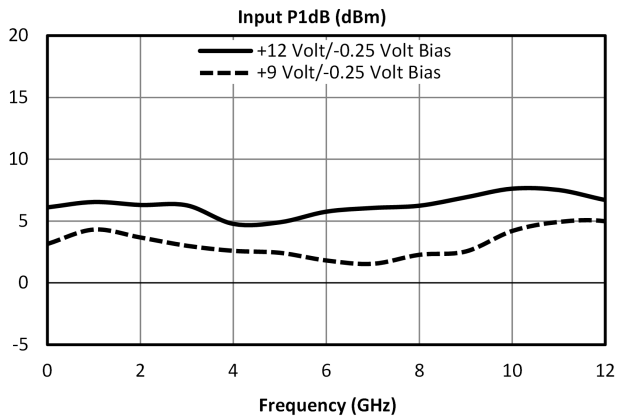
**Typical Performance Plots – +3 to +7V External Bias (Pin 9 Output), -0.25 Negative Bias (Pin 6)**





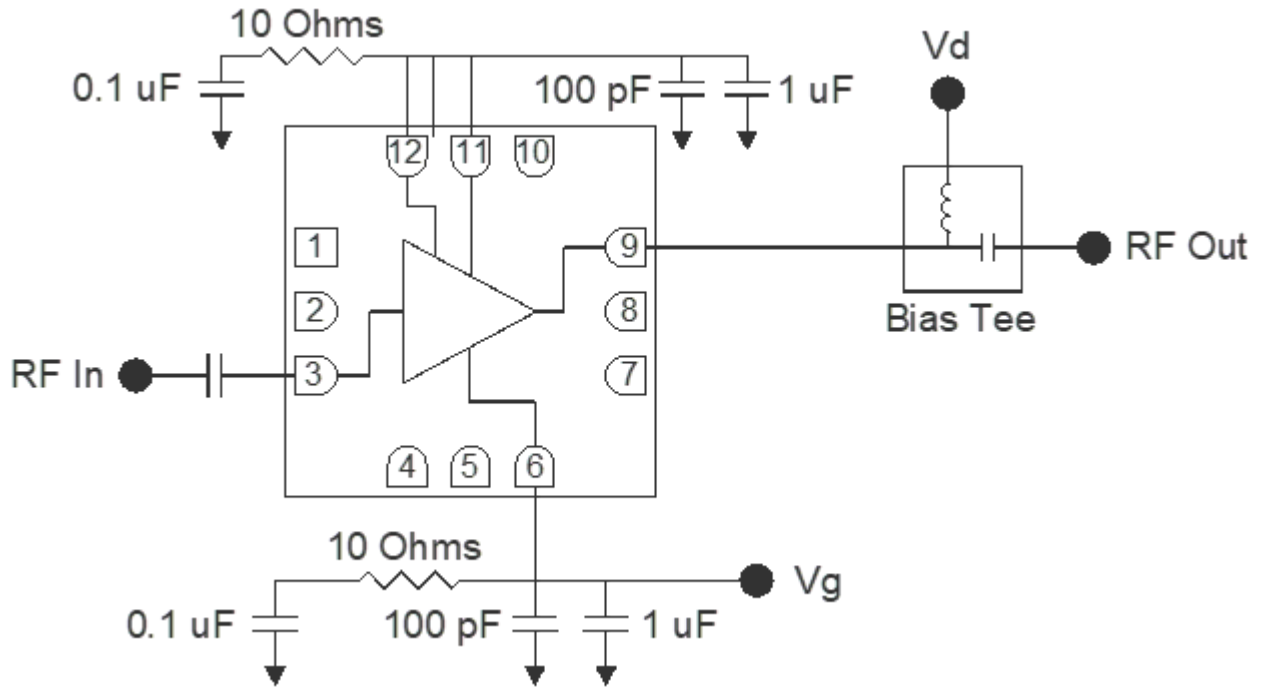
**Typical Performance Plots – +9 to +12V Internal Bias (Pin 11), -0.25 Negative Bias (Pin 6)**





**Application Information**

**Functional Diagram and Application Circuit – External Positive Bias (Pin 9 Output with Bias Tee)**



## **Biasing and Operation**

**RF In / RF Out** – Input and output signals should be connected by 50 ohm microstrip or coplanar traces to well matched 50 ohm sources and loads. DC blocking capacitors or bias tees are required.

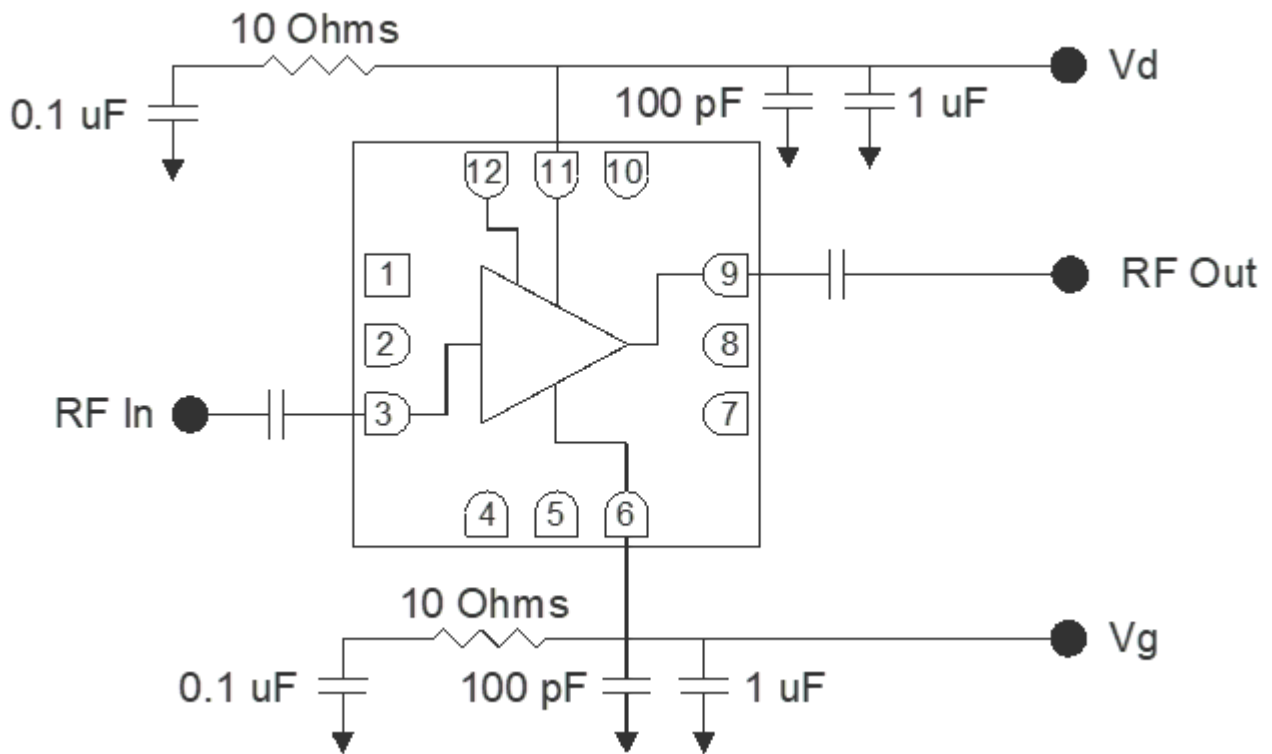
**V<sub>g</sub>** – Negative gate voltage is optional to improve lifetime of the amplifier and reduce current consumption. Harmonic generation is also significantly affected by the negative gate voltage level. The amplifier is designed for optimal performance when the negative gate voltage is tuned such that the positive bias supply is 85 mA. It may be supplied through pin 6 or through the RF input on pin 3.

**Vd**- Bias supply supplied to Vd through pin 9 should be voltage limited below 9 V and current limited below 150 mA at all times. The operational bias voltage should be between 3 V and 7 V for full gain, efficiency, and linearity. In general gain, linearity, and output power will increase marginally with increased voltage from 5 to 7 V.

**Optional Bias Circuitry** – The resistor and capacitor on the Vd and Vg lines (pads 11, 12, and 6) prevent low frequency oscillation. These components are not required in bias circuits with sufficient low frequency loss. Designers should experiment to determine if they are necessary.

**DC/RF Ground** – The ground paddle of the QFN should be connected to a low noise RF and DC ground with very low electrical and thermal resistance for high frequency operation and thermal heat sinking.

**Functional Diagram and Application Circuit – Internal Positive Bias Tee (Pin 11)**



## **Biasing and Operation**

**RF In / RF Out** – Input and output signals should be connected by 50 ohm microstrip or coplanar traces to well matched 50 ohm sources and loads. DC blocking capacitors are required.

**V<sub>g</sub>** – Recommended bias on this pin is -0.1 to -0.3 Volts. Harmonic generation is significantly affected by the negative gate voltage level. The amplifier is designed for optimal performance when the negative gate voltage is tuned such that the positive bias supply is 85 mA. It may be supplied through pin 6 or through the RF input on pin 3.

**Vd**- Bias supply on Vd through pin 11 should be voltage limited below 13 V and current limited below 150 mA at all times. The operational bias voltage should be between 10 V and 12 V for full gain, efficiency, and linearity. In general gain, linearity, and output power will increase marginally with increased voltage from 10 V to 12 V. When the internal positive bias tee is used, pin 12 is left DC and RF open circuited and should not be connected to ground.

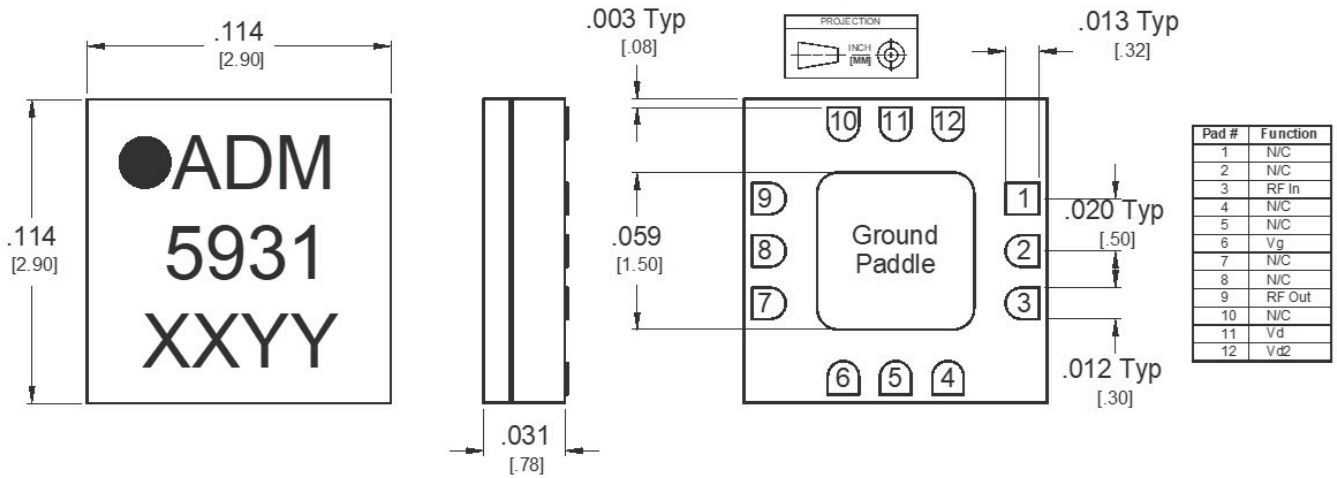
**Optional Bias Circuitry** – The resistor and capacitor on the Vd and Vg lines (pads 11, 12, and 6) prevent low frequency oscillation. These components are not required in bias circuits with sufficient low frequency loss. Designers should experiment to determine if they are necessary.

**DC/RF Ground** – The ground paddle of the QFN should be connected to a low noise RF and DC ground with very low electrical and thermal resistance for high frequency operation and thermal heat sinking.

**Mechanical Data**

**Outline Drawing**

Download : [Outline 3D Drawing](#) | [Outline 3D STP](#)



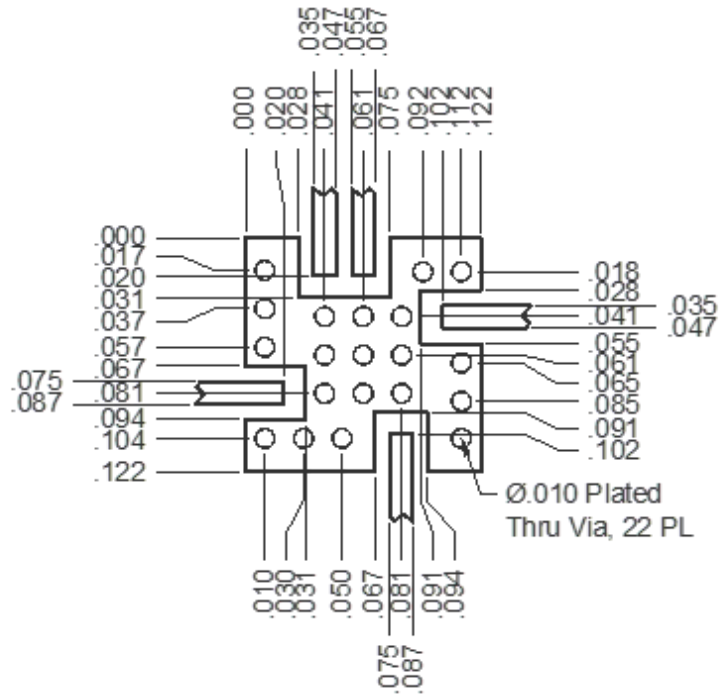
Substrate material is Ceramic.

I/O Leads and Ground Paddle are 1.4±0.6 microns (55±24 micro-inches) Au over 1.3 microns (51 micro-inches) Ni.

All unconnected pads should be connected to PCB RF ground.

**Footprint Image**

Download : [Footprint Drawing](#)



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