

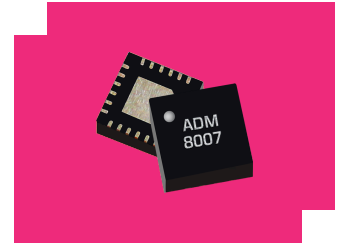
ADM-8007PSM

2 - 40 GHz Surface Mount Amplifier

DEVICE OVERVIEW

General Description

The ADM-8007PSM is a high-linearity, high gain, low noise distributed amplifier capable of providing +23 dBm output power up to 38 GHz. When driven with an input power of 0 to +5 dBm, the ADM-8007PSM can provide sufficient LO drive to power all H and most S diode mixers to 40GHz. The amplifier has excellent return losses and gain flatness.



[Download s-parameters here](#)

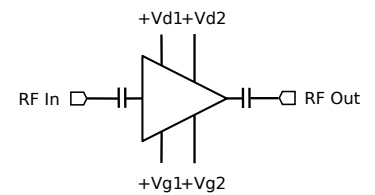
Features

- +24 dBm output power
- +23 dB gain
- 4dB Noise Figure
- Excellent gain flatness
- No negative bias or bias sequencing
- No external bias tee required

Applications

- Mobile test and measurement equipment
- Radar
- SATCOM
- 5G transceivers
- Driver Amplifier for H and S - Diode Mixers

Functional Block Diagram



Part Ordering Options

Part Number	Description	Package	Packing Size	Green Status	Product Lifecycle	Export Classification
ADM-8007PSM	2 - 40 GHz Surface Mount Amplifier	QFN	-	REACH RoHS	Released	3A001.b.2.d
<u>EVB-ADM-8007P</u>	Evaluation Board, 2 - 40 GHz Surface Mount Amplifier	EVB	-	REACH RoHS	Released	EAR99
<u>ADM-8007P-TR</u>	Tape and Reel, 2 - 40 GHz Surface Mount Amplifier	QFN	7"	REACH RoHS	Released	3A001.b.2.d

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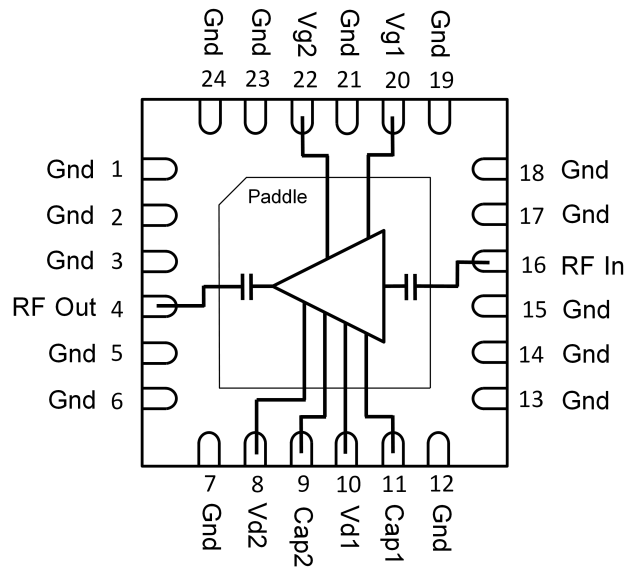
Revision History

Revision Code	Revision Date	Comment
-	2022-09-01	Initial Release
A	2022-10-01	Package Drawing Updated

Port Configuration and Functions

Port Diagram

A port diagram of the ADM-8007PSM QFN package is shown below (X-ray view from the top). The pin functions are detailed in this datasheet.



Port Functions

Port	Function	Description	DC Equivalent Circuit
10	Vd1	Pin 10 is the DC supply pin for the amplifier's input stage.	-
11	Cap1	Pin 11 provides an off-chip AC ground for the input stage. This pin may be left OPEN but should NOT be connected GND. Leaving this pin OPEN will cause some degradation in gain and linearity below 5GHz.	-
1-3, 5-7, 12-15, 17-19, 21, 23, 24	NC	These pins are not internally connected. Datasheet performance is measured with these pins connected to PCB RF ground.	-
16	RF Input	Pin 16 is the amplifier RF input. This pin is internally DC blocked and RF matched to 50 Ohms.	-
20	Vg1	Pin 20 provides bias for an internal current mirror that sets the current draw for amplifier input stage. Increasing current will increase gain at the expense of efficiency. The default series resistor (270 Ohms) is chosen to optimize gain, output power and efficiency when Vg1 and Vd1 are both tied to 5V.	-
22	Vg2	Pin 22 provides bias for an internal current mirror that sets the current draw for amplifier output stage. Increasing current will increase gain at the expense of efficiency. The default series resistor (82.5 Ohms) is chosen to optimize gain, output power and efficiency when Vg2 and Vd2 are both tied to 5V.	-
4	RF Output	Pin 4 is the amplifier RF output. This pin is internally DC blocked and RF matched to 50 Ohms.	-
8	Vd2	Pin 8 is the DC supply pin for the amplifier's output stage.	-
9	Cap2	Pin 9 provides an off-chip AC ground for the output stage. This pin may be left OPEN but should NOT be connected GND. Leaving this pin OPEN will cause some degradation in gain and linearity below 5GHz.	-
Paddle	Ground	The package ground paddle must be connected to a DC/RF ground potential with high thermal and electrical conductivity.	-

Specifications

Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If any one of these limits are exceeded, the device may become inoperable or have a reduced lifetime. Reliability limits are individual, instantaneous catastrophic limits only. Functional operation limits are indicated below. Operation of the device at multiple absolute maximum limits or for extended periods at a single limit can cause degradation and damage to the device.

Parameter	Maximum Rating	Unit
Bias Current (I _g)	95	mA
Bias Voltage (V _g)	8	V
Drain Current (I _d)	400	mA
Drain Supply Voltage (V _d)	8	V
Maximum Operating Temperature for MTTF of 1E6 hours at 85°C Baseplate Temperature	85	°C
Maximum Storage Temperature	125	°C
Max Junction Temperature for MTTF of 1E6 hours at 85°C Baseplate Temperature	175	°C
Max Power Dissipation for MTTF of 1E6 hours at 85°C Baseplate Temperature	1.6	W
Minimum Operating Temperature for MTTF of 1E6 hours at 85°C Baseplate Temperature	-40	°C
Minimum Storage Temperature	-65	°C
RF Input Power	15	dBm
θ _{Jc} , Junction to Case Thermal Resistance	30	°C/W

Package Information

Parameter	Details	Rating
ESD	50 to < 125 Volts	HBM 0A
Weight	Package name: QFN	0.041g
Dimensions	-	4 x 4 mm
Moisture Sensitivity Level	-	MSL 1

Recommended Operating Conditions

The Recommended Operating Conditions indicate the limits, inside which the device should be operated, to guarantee the performance given in Electrical Specifications. Operating outside these limits may not necessarily cause damage to the device, but the performance may degrade outside the limits of the electrical specifications. For limits, above which damage may occur, see Absolute Maximum Ratings.

Parameter	Min	Nominal	Max	Unit
Ambient Temperature	-40	25	85	°C
Power Supply DC Voltage (V _d)	3	5	6	V
Power Supply DC Voltage (V _g)	3	5	6	V
Power Supply DC Current (I _d) (No RF Input) ¹	121	218	259	mA
Power Supply DC Current (I _g) (No RF Input) ²	11	19	23	mA
Input Power for Saturation	0	1	8	dBm

^[1] Recommended operating current conditions without RF input applied. Bias current into V_d pin.

^[2] Recommended operating current conditions without RF input applied. Bias current into V_g pin.

Sequencing Requirements

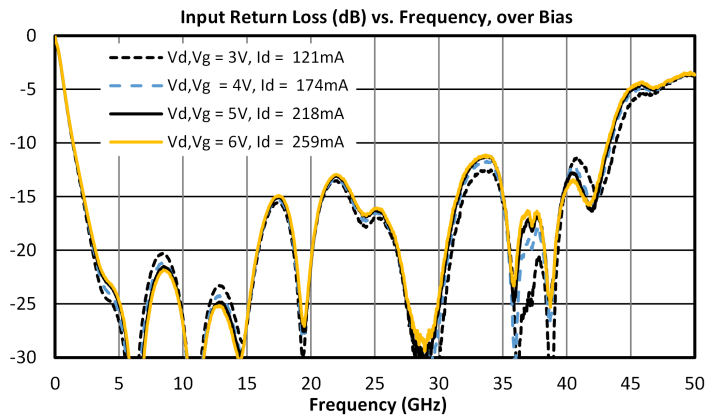
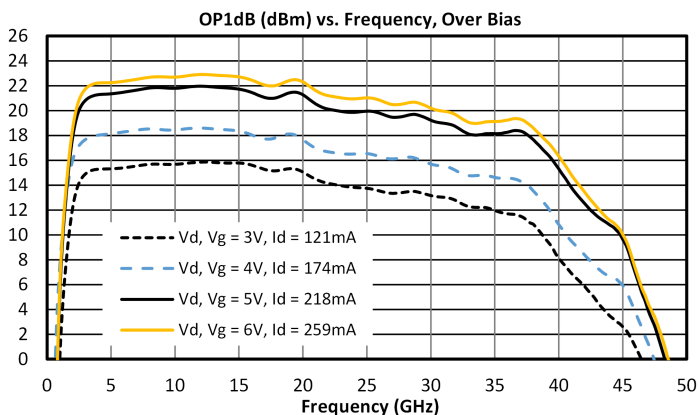
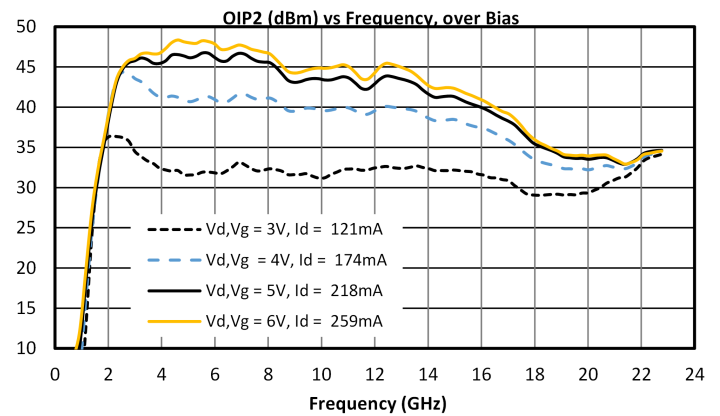
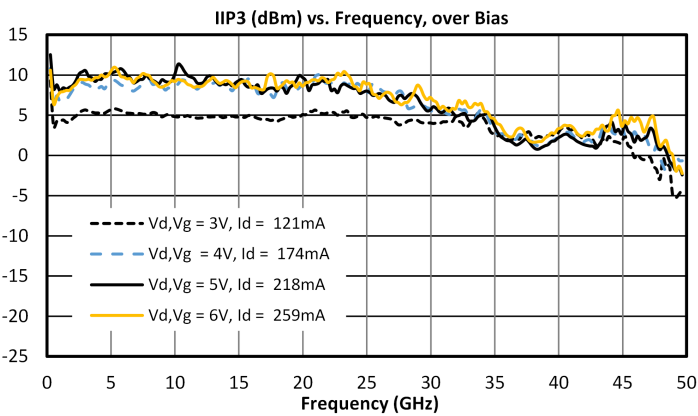
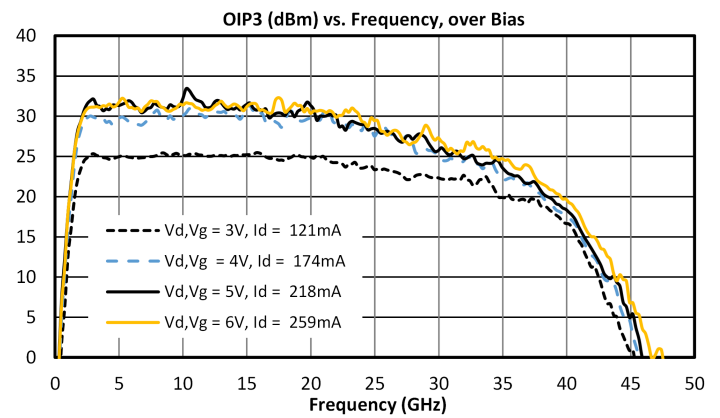
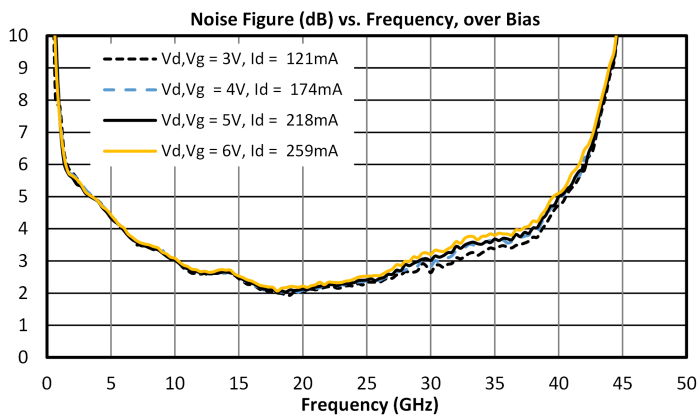
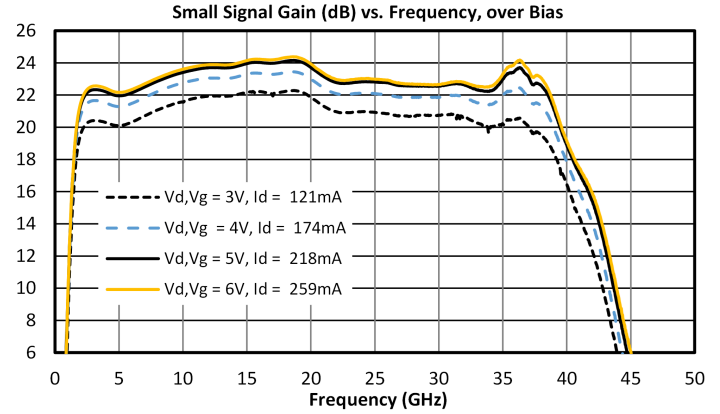
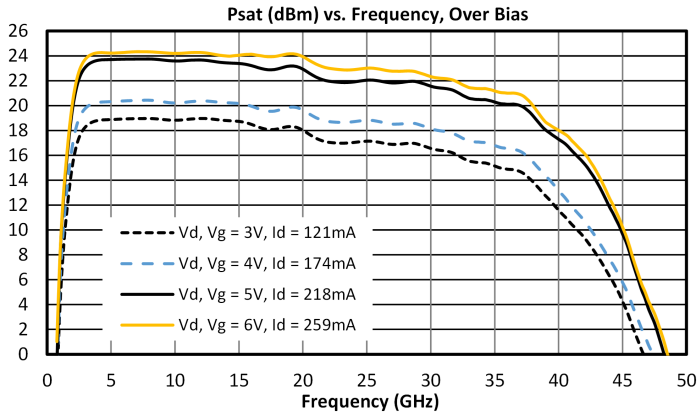
There is no sequencing required to power up or power down the amplifier. The amplifier must have an output load connected during operation.

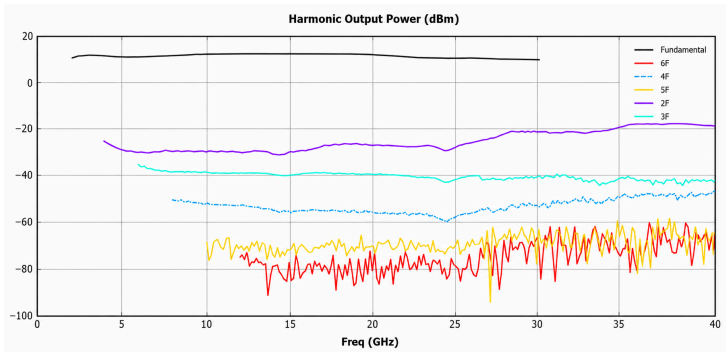
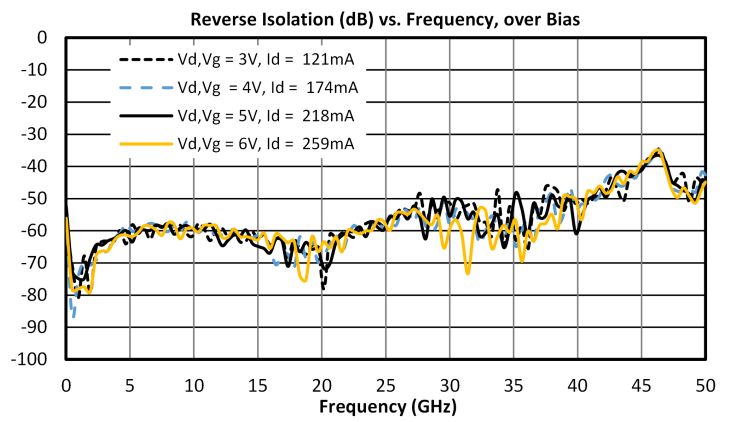
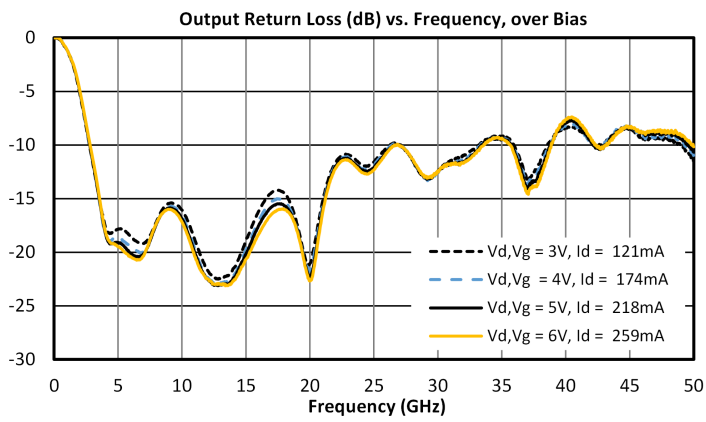
Electrical Specifications

Unless otherwise specified, electrical specifications apply at TA=+25°C, Vd1,Vd2,Vg1,Vg2 = 5 V. Min and Max limits apply only to our connectorized units and are guaranteed at TA=+25°C

Parameter	Test Conditions	Minimum Frequency (GHz)	Maximum Frequency (GHz)	Min	Typ	Max	Unit
Current Consumption	Vd1, Vd2, Vg1, Vg2 = 5 V no RF input	-	-	-	237	-	mA
Input IP3	Vd1, Vd2, Vg1, Vg2 = 5 V Pin = -15 dBm per tone, 10 MHz tone spacing	2	27	-	9	-	dBm
Input IP3	Vd1, Vd2, Vg1, Vg2 = 5 V Pin = -15 dBm per tone, 10 MHz tone spacing	27	40	-	6	-	dBm
Input Power for Saturation	Vd1, Vd2, Vg1, Vg2 = 5 V	2	27	-	2	-	dBm
Input Power for Saturation	Vd1, Vd2, Vg1, Vg2 = 5 V	27	40	-	0	-	dBm
Input Return Loss	Vd1, Vd2, Vg1, Vg2 = 5 V Pin = -20 dBm	2	40	-	20	-	dB
Noise Figure	Vd1, Vd2, Vg1, Vg2 = 5 V Pin = -20 dBm	2	40	-	4	-	dB
Output IP2	Vd1, Vd2, Vg1, Vg2 = 5 V Pin = -15 dBm per tone, 10 MHz tone spacing	12	22	-	37	-	dBm
Output IP2	Vd1, Vd2, Vg1, Vg2 = 5 V Pin = -15 dBm per tone, 10 MHz tone spacing	2	12	-	45	-	dBm
Output IP3	Vd1, Vd2, Vg1, Vg2 = 5 V Pin = -15 dBm per tone, 10 MHz tone spacing	2	27	-	30	-	dBm
Output IP3	Vd1, Vd2, Vg1, Vg2 = 5 V Pin = -15 dBm per tone, 10 MHz tone spacing	27	40	-	25	-	dBm
Output P1dB	Vd1, Vd2, Vg1, Vg2 = 5 V	2	27	-	19	-	dBm
Output P1dB	Vd1, Vd2, Vg1, Vg2 = 5 V	27	40	-	16	-	dBm
Output Return Loss	Vd1, Vd2, Vg1, Vg2 = 5 V Pin = -20 dBm	2	40	-	15	-	dB
Reverse Isolation	Vd1, Vd2, Vg1, Vg2 = 5 V Pin = -20 dBm	2	40	-	50	-	dB
Saturated Output Power	Vd1, Vd2, Vg1, Vg2 = 5 V	2	27	-	23	-	dBm
Saturated Output Power	Vd1, Vd2, Vg1, Vg2 = 5 V	27	40	-	21	-	dBm
Small Signal Gain	Vd1, Vd2, Vg1, Vg2 = 5 V Pin = -20 dBm	2	40	-	23	-	dB

Typical Performance Plots





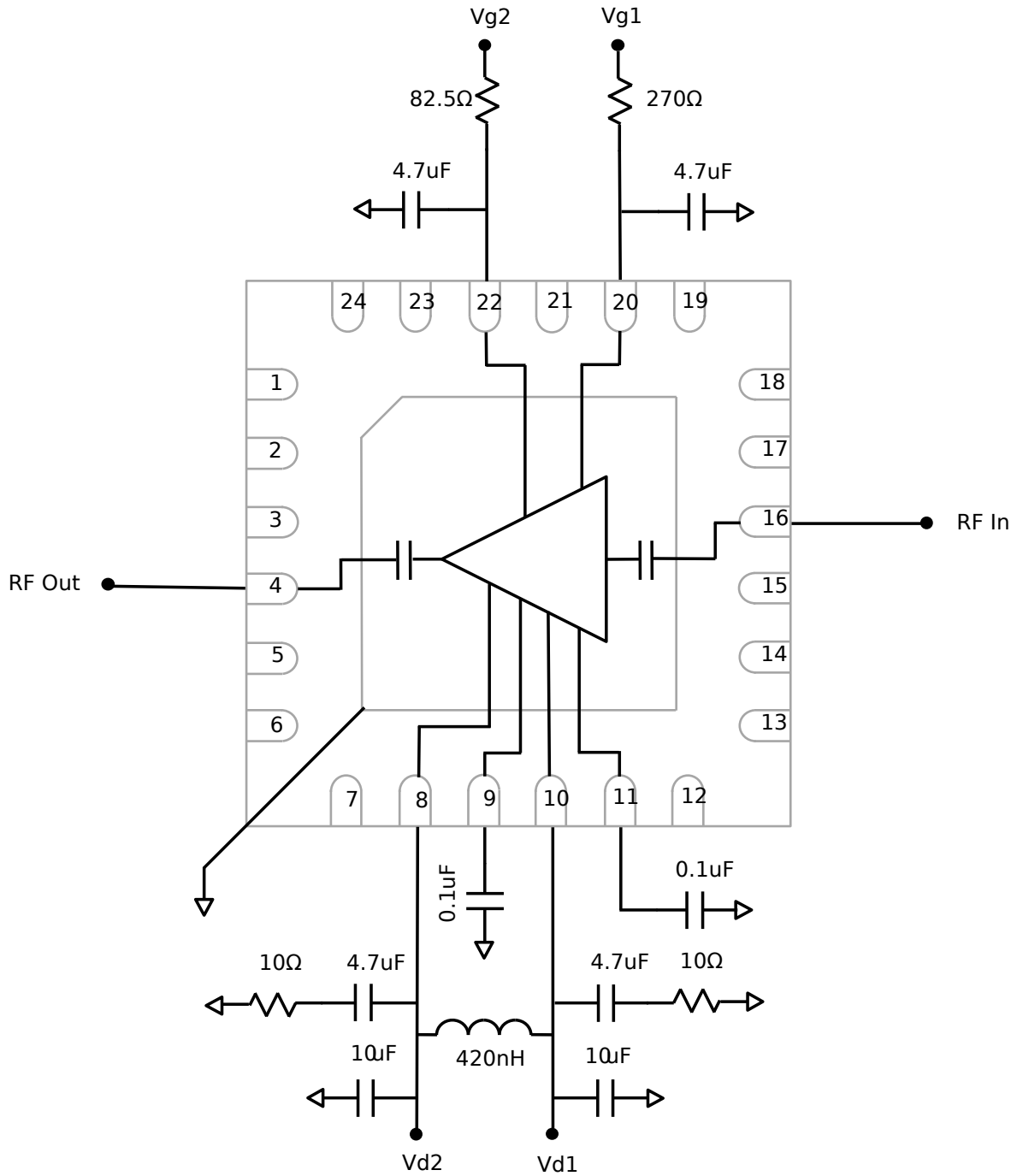
Application Information

Application Circuit

Below are the recommended application circuits for the ADM-8007PSM. The resistors connected along the Vg1 and Vg2 pathways are there to set the bias currents as shown in the performance plots in the previous section. Customers can choose to adjust these values based on their specific application's performance and power requirements. In general, increasing the values of these resistors will reduce current consumption on both the Vd and Vg lines, but will reduce gain and will have a slight impact on other performance parameters compared to those shown in the previous section.

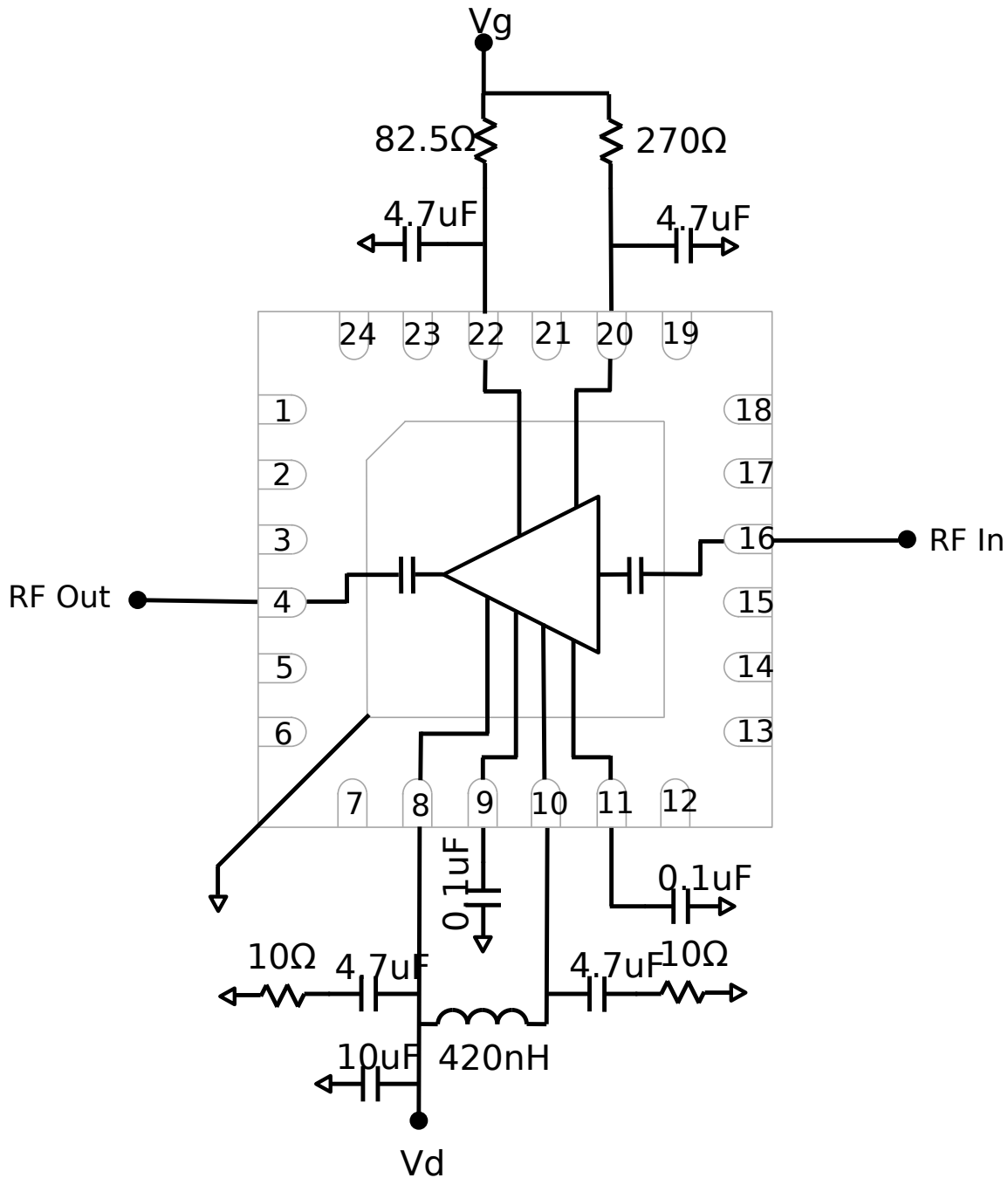
Application Circuit (Independent Supplies)

The application circuit below is provided for independent Vd1 and Vd2 sources.



Application Circuit (Single DC Supply)

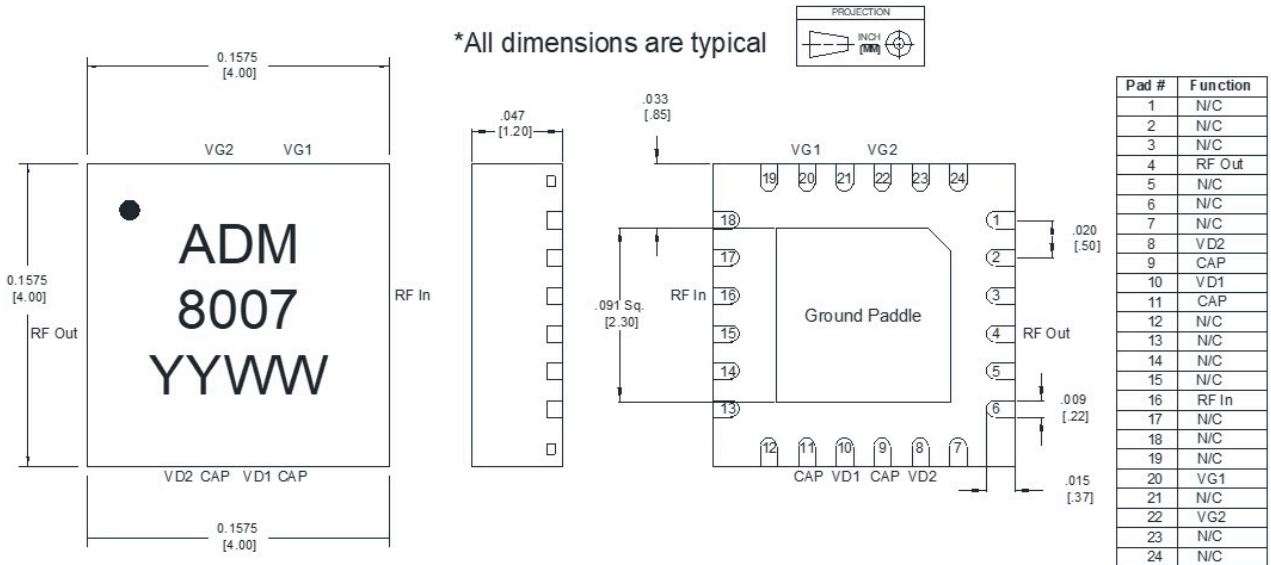
The circuit below is recommended for applications using a single DC power supply. When Vd1 and Vd2 are provided from a single supply and a single trace near the amp, extra isolation is required between Vd1 and Vd2 pins to guarantee stability. In the circuit below, this is accomplished with the 420nH series inductor to Vd1. The inductor should be placed on the Vd1 supply to limit IR drop due to higher current draw on the Vd2 line.



Mechanical Data

Outline Drawing

Download : [Outline 2D Drawing](#) | [Outline 3D Drawing](#) | [Outline 3D STP](#)

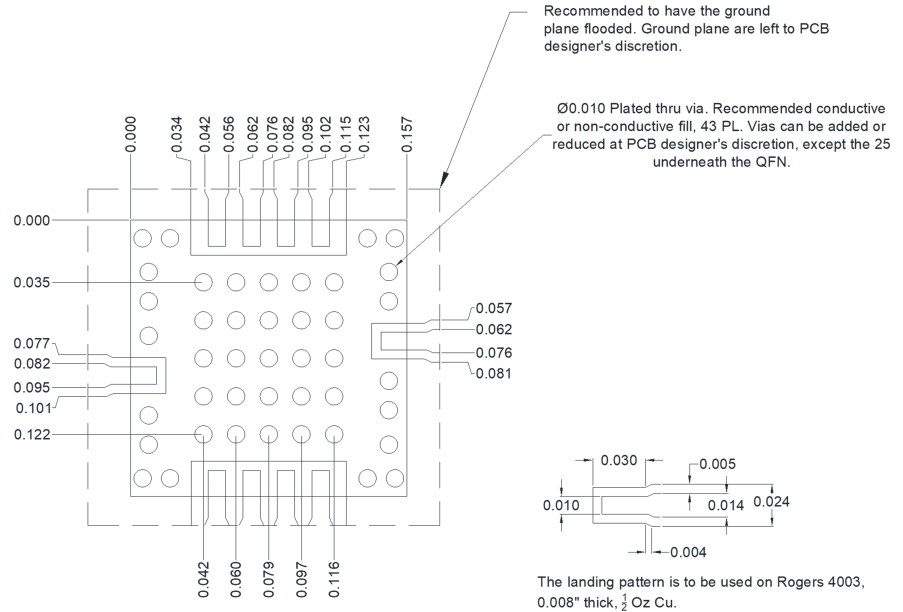
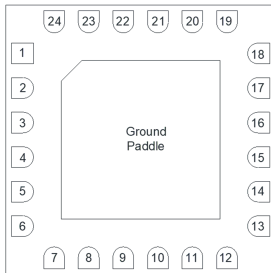


- 1) Substrate material is LCP
- 2) I/O Leads and Die Paddle is (from base to finish):
 - a. Ni: 0.5 um MIN
 - b. Pd: 0.02 um MIN
 - c. Au: 0.05 um MAX
- 3) All unconnected pins should be connected to PCB RF ground.

Footprint Image

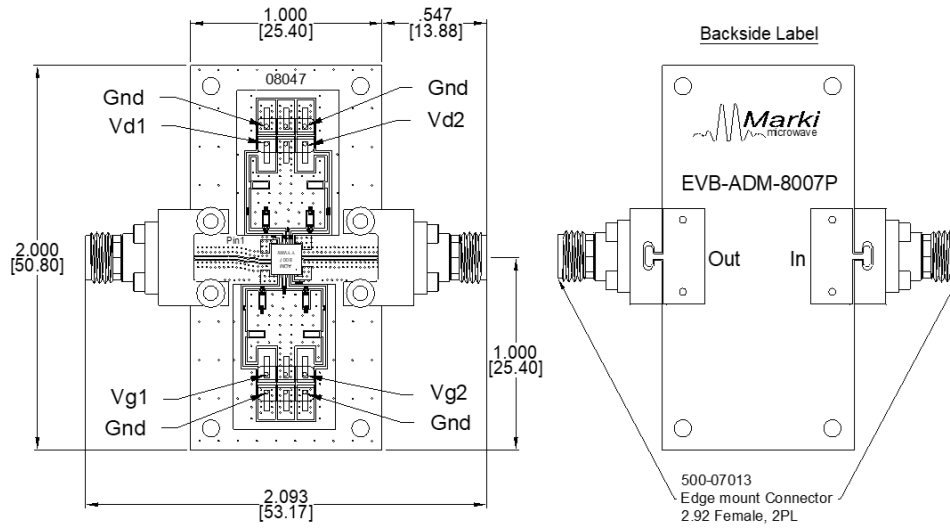
Download : [Footprint Drawing](#)

QFN 4mm Sample Drawing
X-Ray view



Evaluation Board - Outline Drawing

All Dimensions are typical.



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