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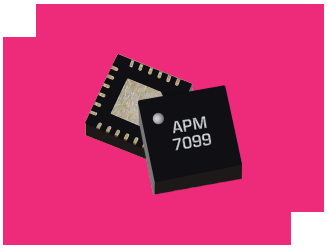
APM-7099SM

0.01-20 GHz Surface Mount Low Phase Noise Amplifier

DEVICE OVERVIEW

General Description

The APM-7099SM is a broadband low phase noise driver amplifier designed to provide a saturated +25 dBm output power with low DC power consumption. This amplifier uses GaAs HBT technology for low phase noise, and is optimized to drive our NLTL multiplier line. It can also provide enough power to drive the LO port of an S-diode mixer from 10 MHz to 15 GHz, or of an H or L-diode mixer from 10 MHz to 20 GHz. This amplifier can be operated with a variety of bias conditions for both low and high-power applications. The APM-7099SM is packaged in a compact 4 mm QFN for surface mount integration on circuit board-based systems.



Download s-parameters here

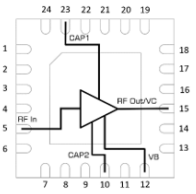
Features

- -167 dBc/Hz phase noise at 10 kHz offset frequency
- +25 dBm output power up to 20GHz
- Low DC power consumption
- Positive-only biasing
- No sequencing required
- Unconditionally stable

Applications

- Mobile test and measurement equipment
- Radar and satellite communications
- 5G transceivers
- Driver amplifier L,H,S – diode mixers
- NLTL Driver
- Suitable as a T3 driver

Functional Block Diagram



Part Ordering Options

Part Number	Description	Package	Packing Size	Green Status	Product Lifecycle	Export Classification
APM-7099SM	0.01-20 GHz Surface Mount Low Phase Noise Amplifier	QFN	-	REACH RoHS	Released	EAR99
EVAL-APM-7099SM	Evaluation Board, 0.01-20 GHz Surface Mount Low Phase Noise Amplifier	EVAL	-	REACH RoHS	Released	EAR99
APM-7099SM-TR	Tape and Reel, 0.01-20 GHz Surface Mount Low Phase Noise Amplifier	QFN	7"	REACH RoHS	Released	EAR99

Table Of Contents

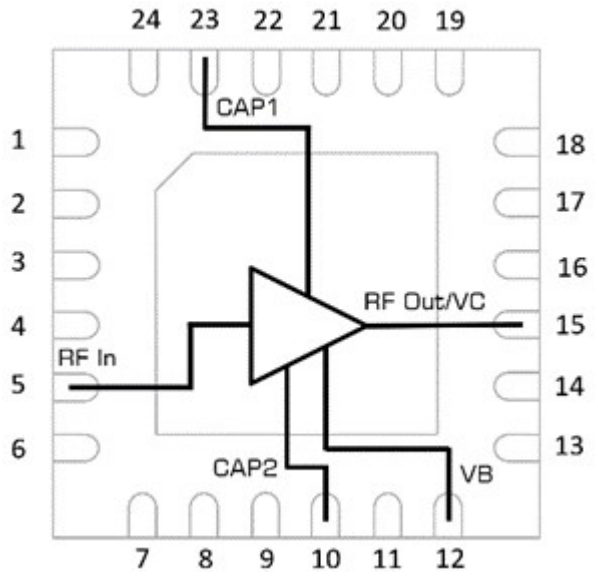
Revision History

Revision Code	Revision Date	Comment
-	2020-10-01	Datasheet Initial Release
A	2021-02-01	Updated Thermal Specs, Absolute Max Table, and Min Specs
B	2021-07-01	Updated Saturated Output Power Min Spec bandwidth
C	2023-03-01	Updated Application Circuit

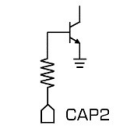
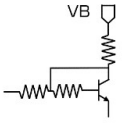
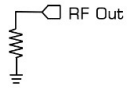
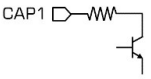
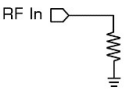
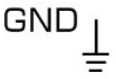
Port Configuration and Functions

Port Diagram

A port diagram of the APM-7099SM is shown below.



Port Functions

Port	Function	Description	Equivalent Circuit for Package
10	Off-Chip Cap Port 2	Port 10 allows the user to attach additional off chip bypass capacitance to provide adequate low frequency AC grounding termination to the input matching network. The value should be at least 100nF.	
12	Current Mirror Bias Port	Port 12 is the DC voltage bias pad for the current mirror that controls the collector current supplied to the amplifier. See APM-7099SM Typical Performance Plots for performance at different bias conditions.	
15	RF Output and Collector Supply Port	This is the amplifier's RF Output and positive VC supply voltage pin. It is RF matched to 50 Ω and is DC coupled. Must have less than 7:1 VSWR when operating.	
23	Off-Chip Cap Port 1	Port 23 allows the user to attach additional off chip bypass capacitance to provide adequate low frequency AC grounding termination to the input matching network. The value should be at least 100nF.	
5	RF Input	This is the RF input port of the device, and is RF matched to 50 Ω. This port is DC-coupled, and requires a blocking capacitor.	
GND	Ground	IC backside must be connected to a DC/RF ground with high thermal and electrical conductivity.	

Specifications

Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If these limits are exceeded, the device may become inoperable or have a reduced lifetime.

Parameter	Maximum Rating	Unit
Bias (Current Mirror) Voltage (VB)	9	V
Maximum Operating Temperature	85	°C
Maximum Storage Temperature	150	°C
Max Junction Temperature for MTTF> 1E6 hours	125	°C
Max Power Dissipation for MTTF of 1E6 hours at 85°C Baseplate Temperature	709	mW
Minimum Operating Temperature	-40	°C
Minimum Storage Temperature	-65	°C
Output Load VSWR	7	-
Power Supply (Collector) Current (Ic)	225	mA
Power Supply (Collector) Voltage (VC)	9	V
RF Input Power (10 MHz – 3GHz)	12	dBm
RF Input Power (3 GHz – 20 GHz)	15	dBm
θJC, Junction to Ambient Thermal Resistance	56	°C/W

Package Information

Parameter	Details	Rating
Dimensions	-	4 x 4 mm
Moisture Sensitivity Level	-	MSL 1

Recommended Operating Conditions

The Recommended Operating Conditions indicate the limits, inside which the device should be operated, to guarantee the performance given in Electrical Specifications Operating outside these limits may not necessarily cause damage to the device, but the performance may degrade outside the limits of the electrical specifications. For limits, above which damage may occur, see Absolute Maximum Ratings.

Parameter	Min	Nominal	Max	Unit
Ambient Temperature	-40	25	85	°C
Quiescent DC Current (Ic)	38	72	132	mA
Input Power for Saturation	10	11	12	dBm
Positive DC Voltage (VC)	5	8	9	V
DC Current with RF Input (Ic)	-	-	225	mA
Positive DC Current Mirror Voltage (VB)	5	7	9	V

Maximum recommended operating current conditions without RF input applied. Please see typical performance plots for relationship between RF input power and DC current draw.

Sequencing Requirements

There is no sequencing required to power up or power down the amplifier.
Amplifier must have an output load connected when operating.

Electrical Specifications

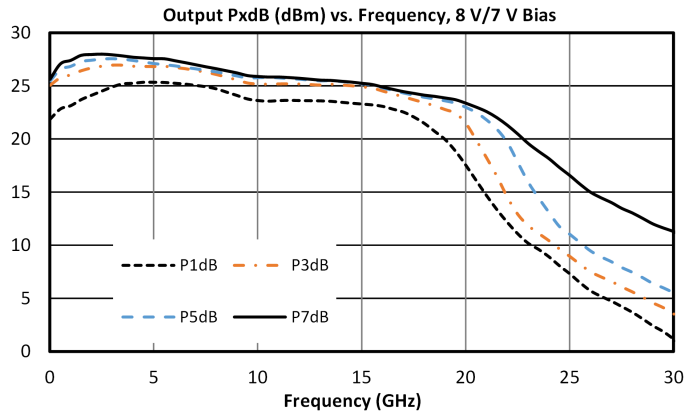
The electrical specifications apply at TA=+25 °C in a 50 Ω system. QFNs are 100% RF tested.

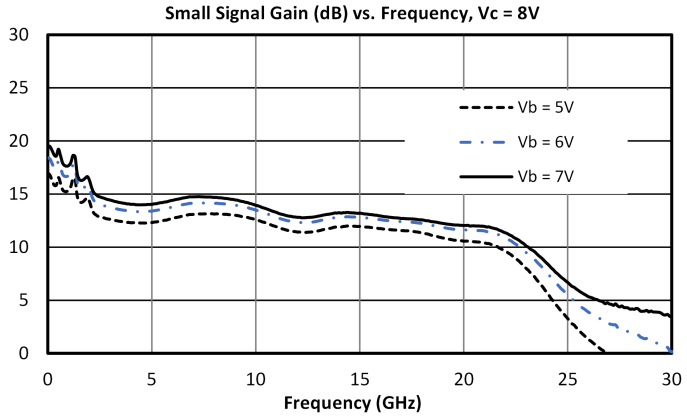
Parameter	Test Conditions	Minimum Frequency (GHz)	Maximum Frequency (GHz)	Min	Typ	Max	Unit
Collector Current, Ic [1]	8 V/6 V	-	-	-	53	-	mA
Collector Current, Ic [2]	8 V/7 V	-	-	-	72	-	mA
Current Mirror Current, Ib	8 V/6 V	-	-	-	3.4	-	mA
Current Mirror Current, Ib	8 V/7 V	-	-	-	4.2	-	mA
Input IP3	8 V/7 V bias, -12 dBm Input Power	0.01	20	-	13	-	dBm
Input Power for Saturation	8 V/7 V bias	0.01	20	-	12	-	dBm
Input Return Loss	8 V/7 V bias, -20 dBm Input Power	0.01	20	-	8	-	dB
Noise Figure	8 V/7 V bias, -20 dBm Input Power	0.01	20	-	6	-	dB
Output IP3	8 V/7 V bias, -12 dBm Input Power	0.01	20	-	27	-	dBm
Output P1dB	8 V/7 V bias	0.01	20	-	21	-	dBm
Output Power [3]	8V/7V bias, P7dB	15	20	-	23	-	dBm
Output Power [4]	8V/7V bias, P7dB	0.01	0.1	-	20	-	dBm
Output Power [5]	8V/7V bias, P7dB	0.1	15	19	25	-	dBm
Output Return Loss	8 V/7 V bias, -20 dBm Input Power	0.01	20	-	12	-	dB
Phase Noise @ 10 kHz Offset	+13 dBm Input power	1	1	-	-167	-	dBc/Hz
Reverse Isolation	8 V/7 V bias, -20 dBm Input Power	0.01	20	-	28	-	dB
Small Signal Gain	8 V/7 V bias, -20 dBm Input Power	0.01	15	10	14	-	dB
Small Signal Gain	8 V/7 V bias, -20 dBm Input Power	15	20	-	12	-	dB

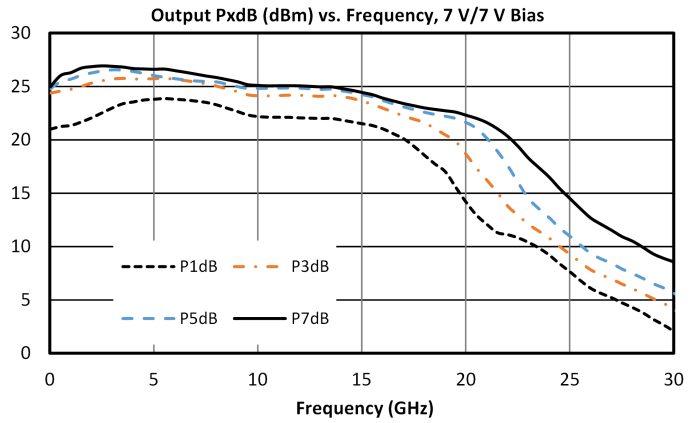
[1][2] Bias conditions for Ic and Ib tested with no RF input power. See APM-7099SM Typical Performance Plots for DC current vs. RF power. Bias conditions presented as VC/VB.
[3][4][5] Saturated output power specification defined using the EVAL-APM-7099SM P7dB compression curve shown in APM-7099SM Typical Performance Plots.

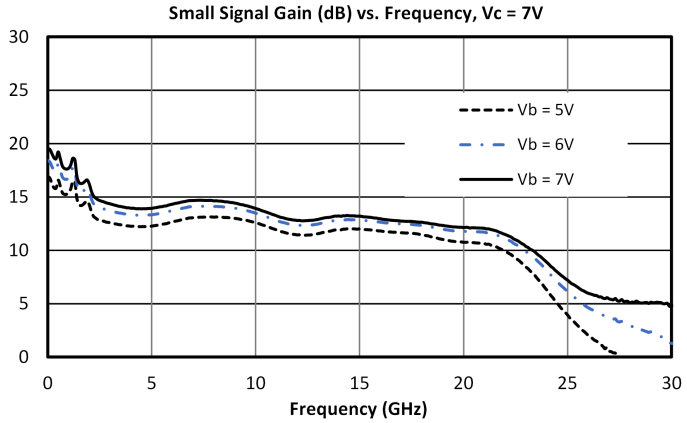
APM-7099SM Typical Performance Plots

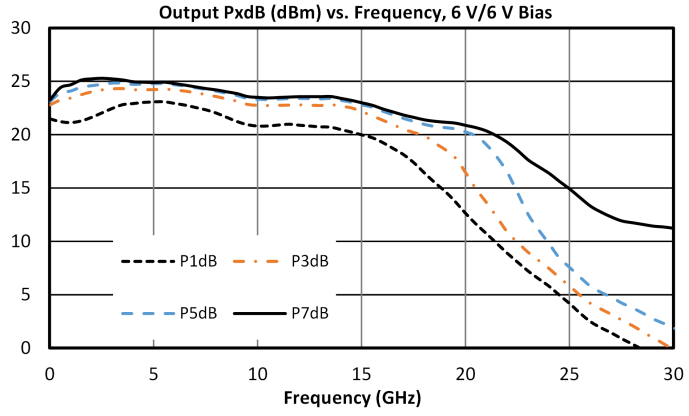
APM-7099SM measurements taken in EVAL-APM-7099SM evaluation board.

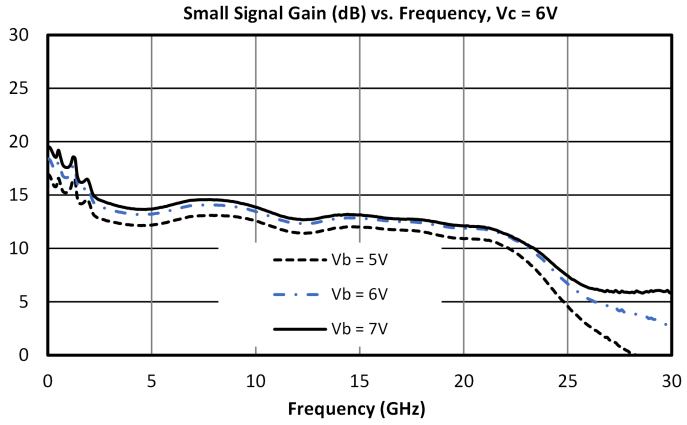








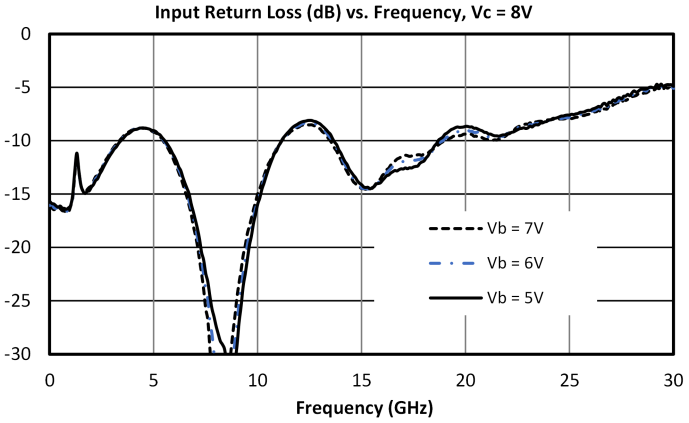




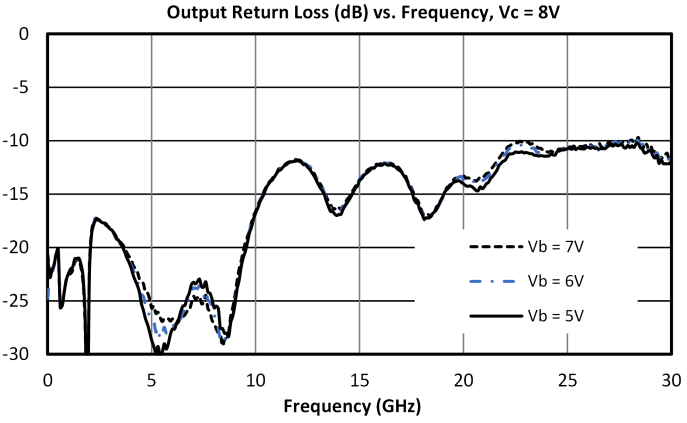
APM-7099SM

0.01-20 GHz Surface Mount Low Phase Noise Amplifier

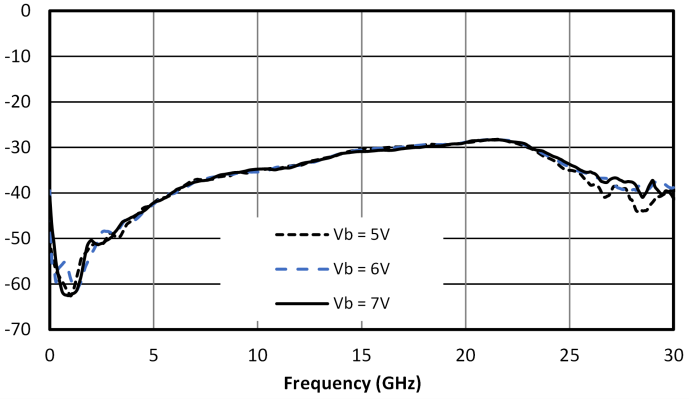
Input Return Loss (dB) vs. Frequency, Vc = 8V



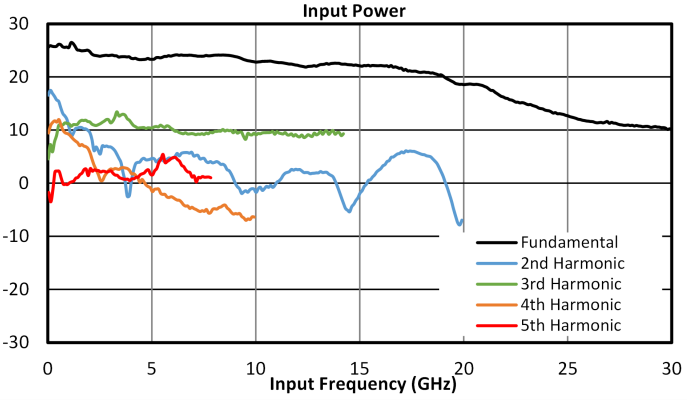
Output Return Loss (dB) vs. Frequency, Vc = 8V



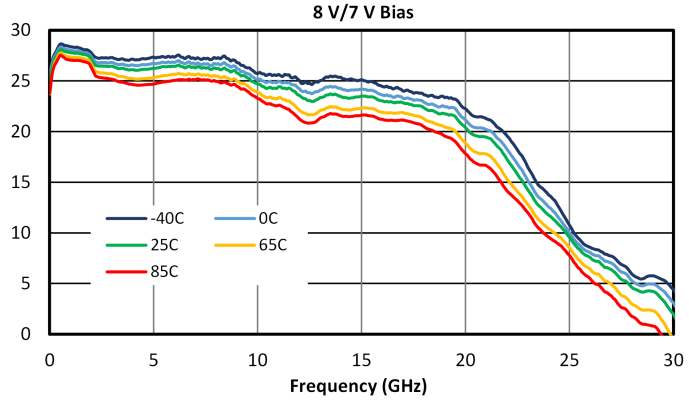
Reverse Isolation (dB) vs. Frequency, Vc = 8V



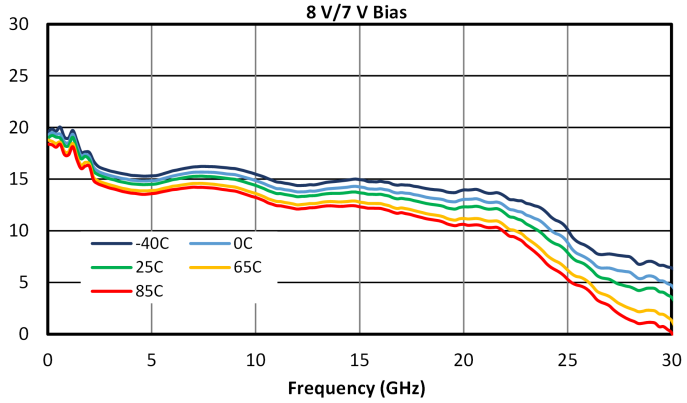
Harmonic Response (dBm) vs. Input Freq. 8 V/8 V Bias, +11 dBm Input Power



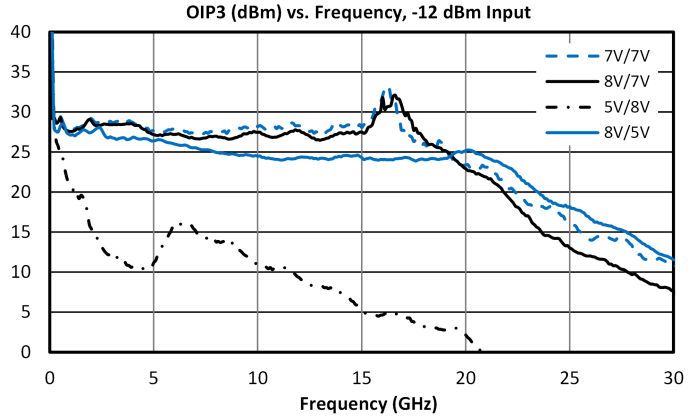
Saturated Output Power (dBm) vs. Frequency over Temperature, 8 V/7 V Bias



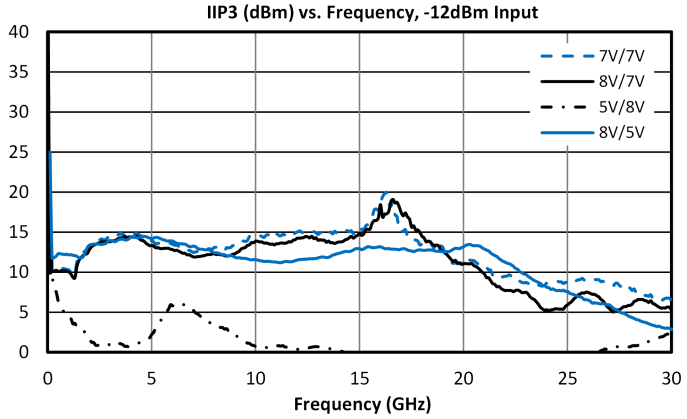
Small Signal Gain (dB) vs. Frequency over Temperature, 8 V/7 V Bias



OIP3 (dBm) vs. Frequency, -12 dBm Input



IIP3 (dBm) vs. Frequency, -12dBm Input



APM-7099SM

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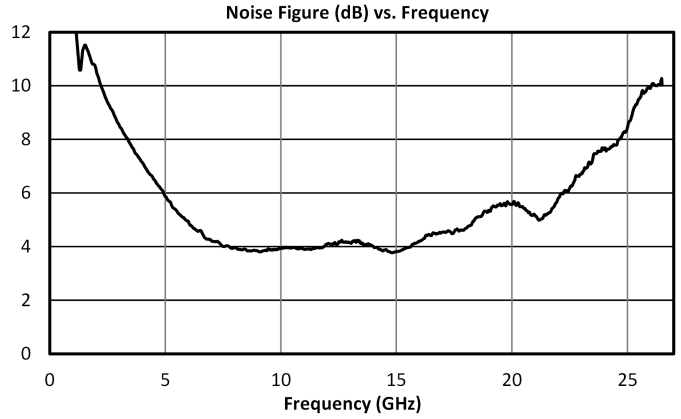
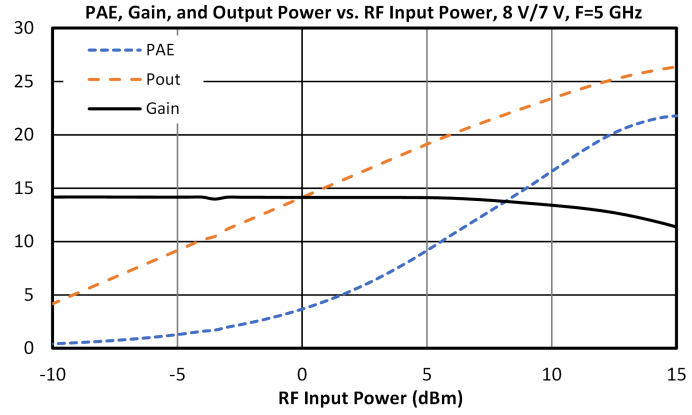
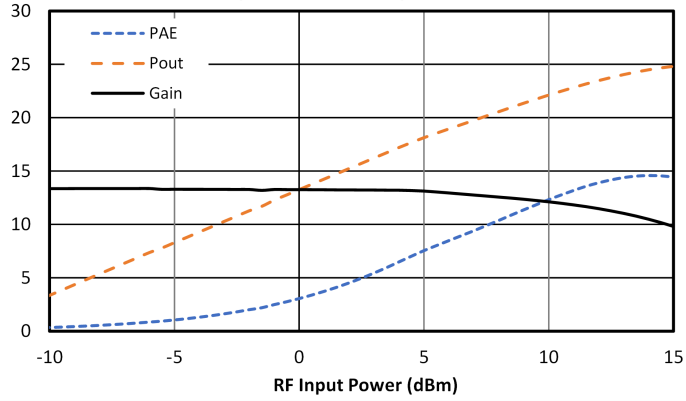
Noise Figure (dB) vs. Frequency



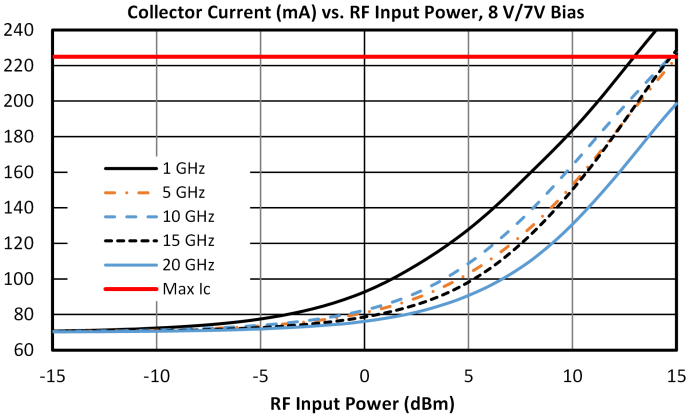
PAE, Gain, and Output Power vs. RF Input Power, 8 V/7 V, F=5 GHz



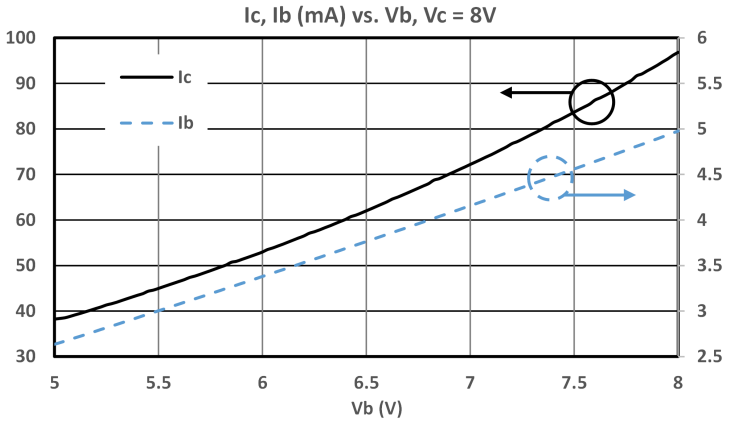
PAE, Gain, and Output Power vs. RF Input Power, 8 V/7 V, F=15 GHz



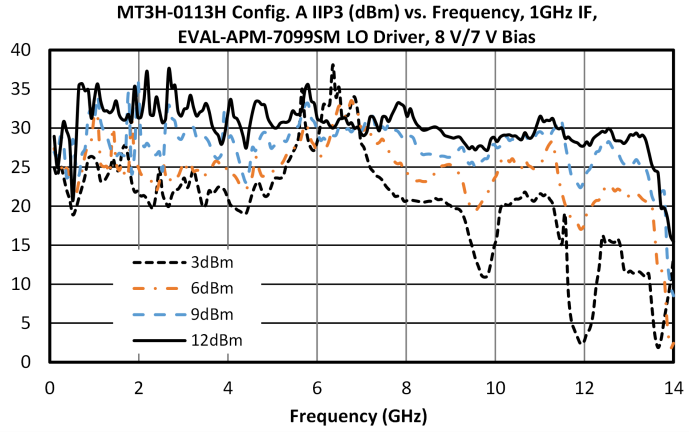
Collector Current (mA) vs. RF Input Power, 8 V/7V Bias

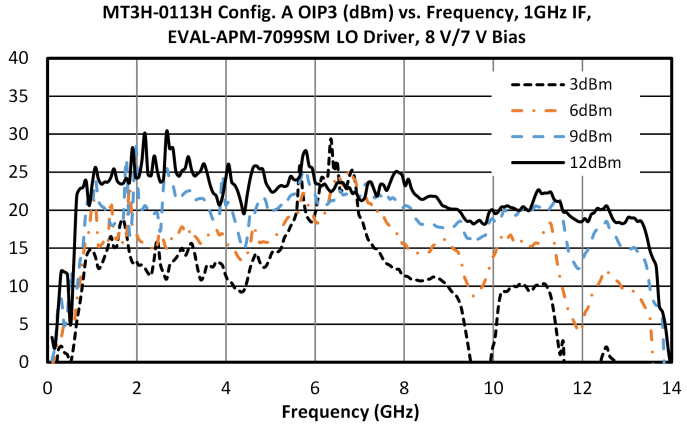


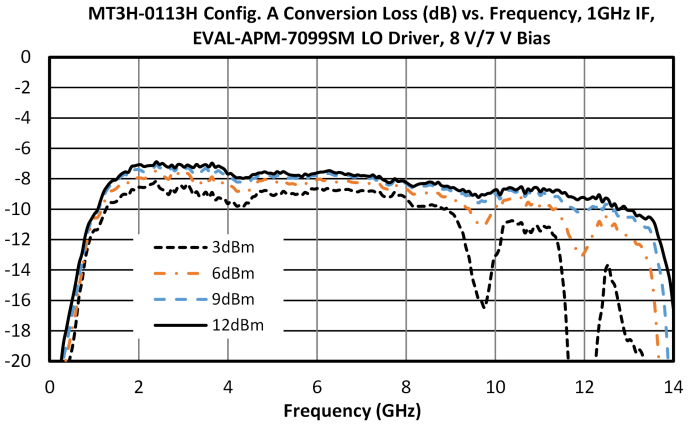
Ic, Ib (mA) vs. Vb, Vc = 8V



Typical Performance Plots of Marki MT3H-0113H Driven With APM-7099SM



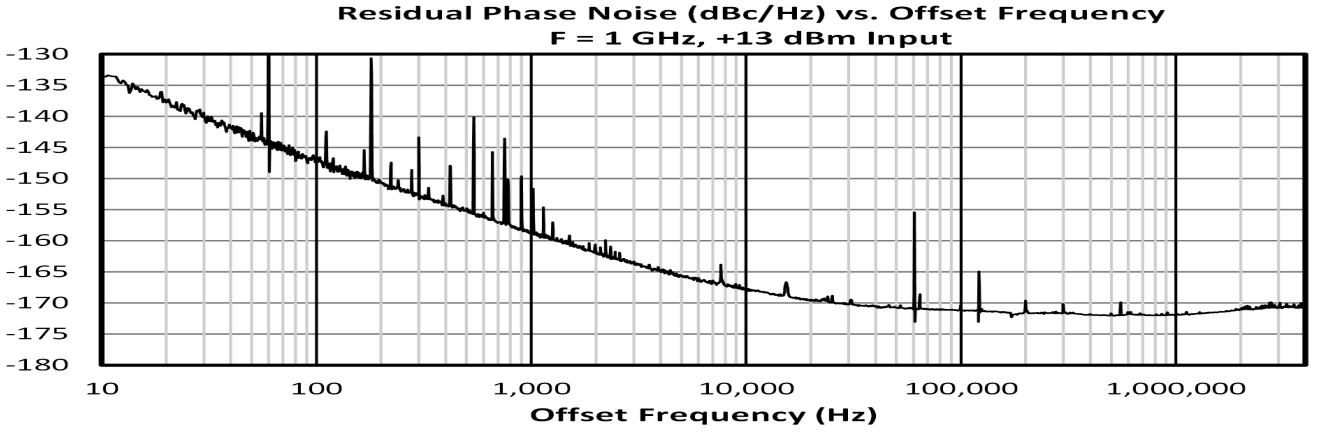




Connectorized Module APM-7099PA Performance Plots

Phase Noise Plot

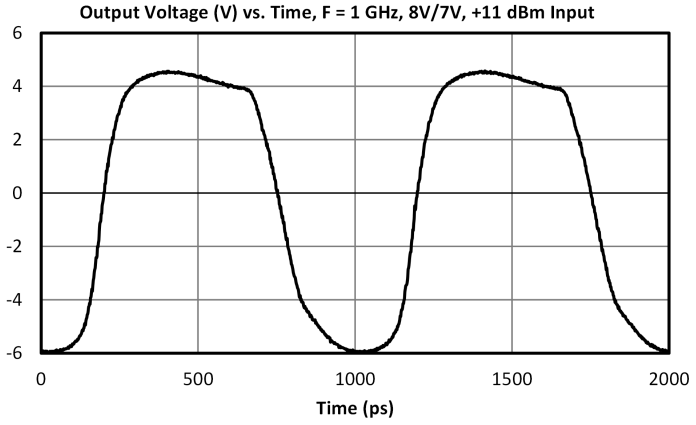
Surface mount module APM-7099SM performance can be expected to be similar to connectorized module performance.

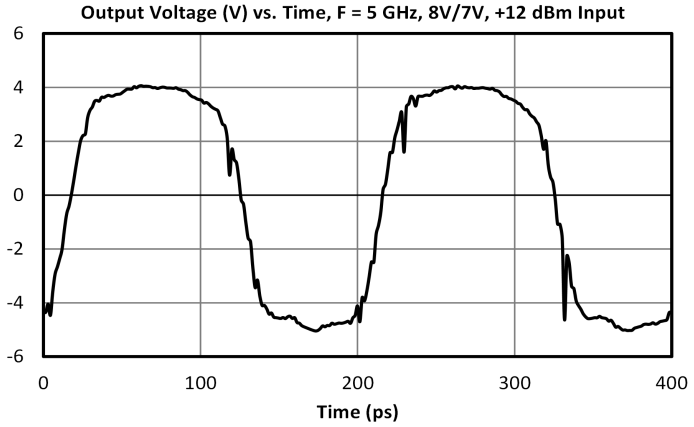


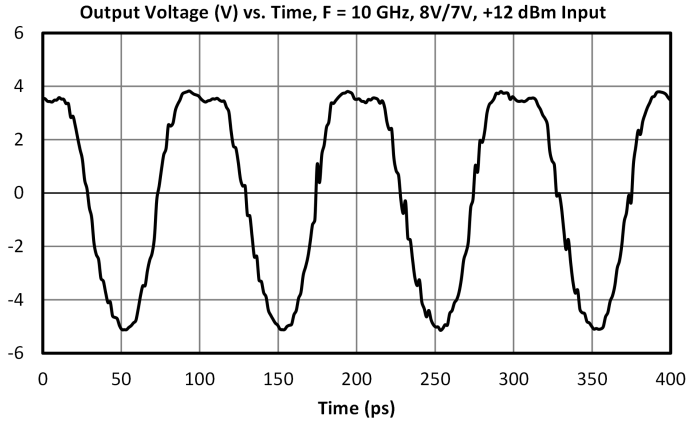
Time Domain Plots

Fast rise time is desirable for linear T3 mixer operation.

Data taken using APM7099PA module





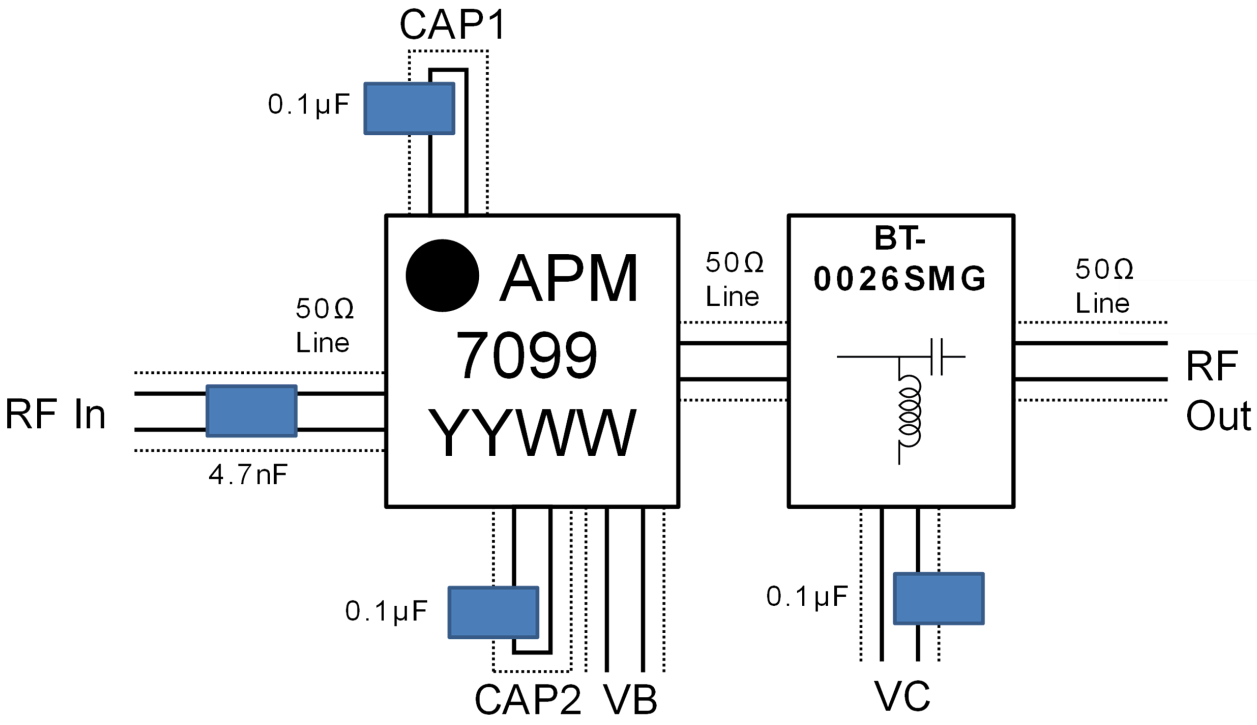


Application Information

APM-7099SM Application Circuit

Below is the recommended application circuit for the APM-7099SM.

Application Circuit



Application Circuit Description

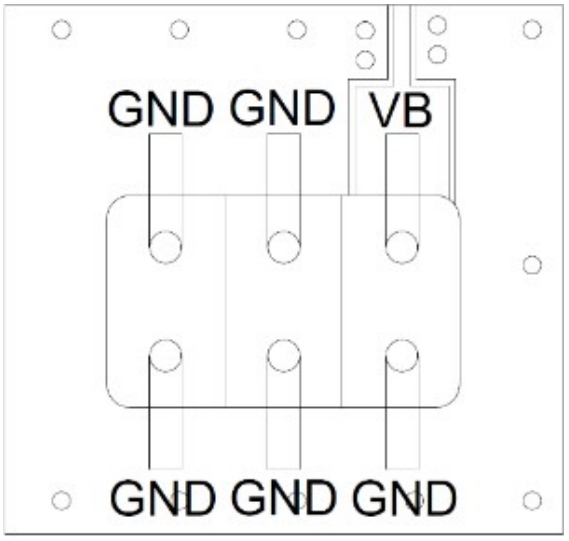
RF input and output should be soldered to 50 Ω traces. A suggested capacitor for the bypass capacitors would be 0402 0.1 uF 16 V surface mount capacitors, such as the AVX 0402YD104KAT2A. For the input blocking capacitor, the suggested capacitor would be a 0402 4.7 nF 16V surface mount capacitor, such as the AVX 0402YD472KAT2A.

Bypass Capacitors

The bypass capacitors on ports CAP1 and CAP2 provide AC ground to the internal circuits on the chip. These should not be DC coupled to prevent disruption of the internal biasing circuits, or outright damage to the chip. The value of these be at least 100nF to provide adequate AC grounding. An additional 100 nF bypass capacitor should be added to the VC line to stabilize the amplifier and prevent power supply feedback to other parts on the board.

Evaluation Board Header Pinout

On the EVAL-APM-7099SM, there is a header for biasing the VB port. Only one pin is connected to VB, all other pins are soldered directly to the top side ground plane.



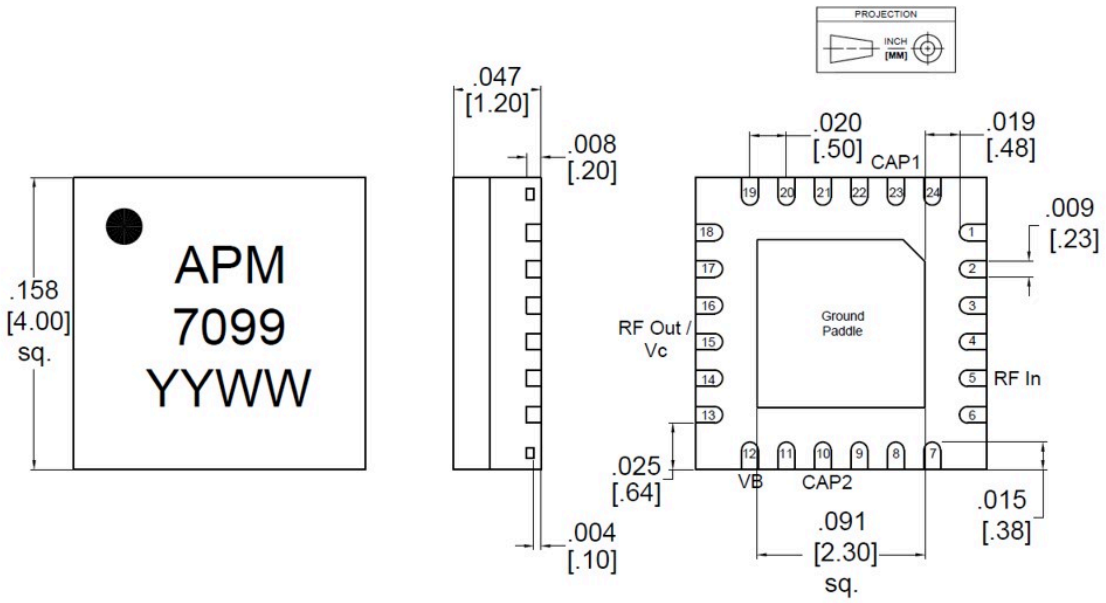
Harmonic Generation

The APM-7099's harmonic generation can be controlled by adjusting the supply and bias voltages. Decreasing the base voltage VB will increase the even harmonic generation and odd harmonic suppression. To increase the odd harmonic generation and even harmonic suppression, decrease the collector voltage VC. The optimal bias condition for even harmonic generation is VC=8 V and VB=5 V, while the optimal bias condition for odd harmonic generation is VC=5 V and VB=8 V.

Mechanical Data

Outline Drawing

Download : Outline 2D Drawing | Outline 3D Drawing | Outline 3D STP

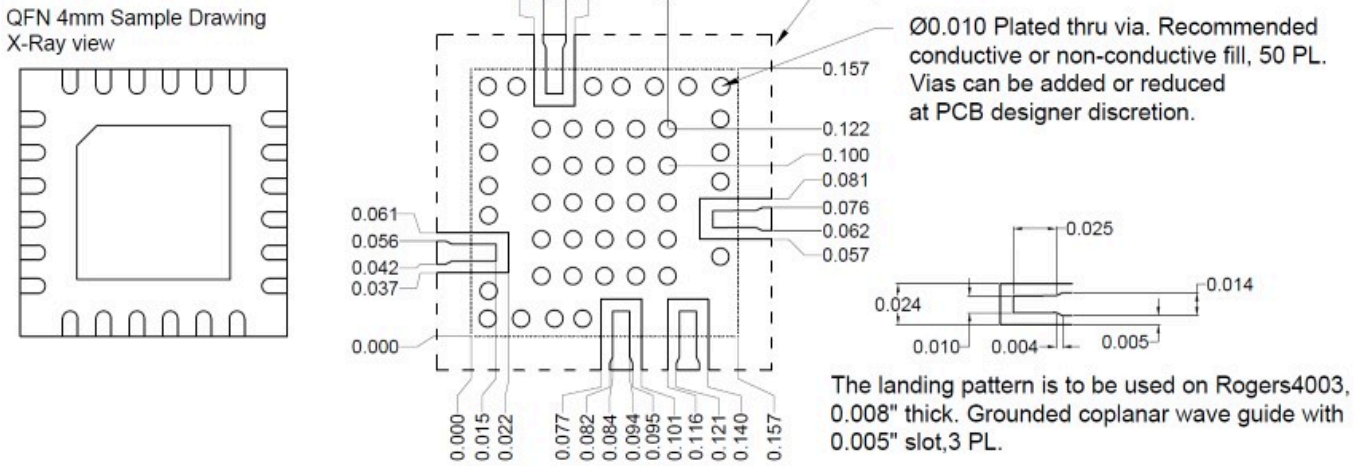


Pad #	Function
1	N/C
2	N/C
3	N/C
4	N/C
5	RF In
6	N/C
7	N/C
8	N/C
9	N/C
10	CAP2
11	N/C
12	VB
13	N/C
14	N/C
15	RF Out / VC
16	N/C
17	N/C
18	N/C
19	N/C
20	N/C
21	N/C
22	N/C
23	CAP1
24	N/C

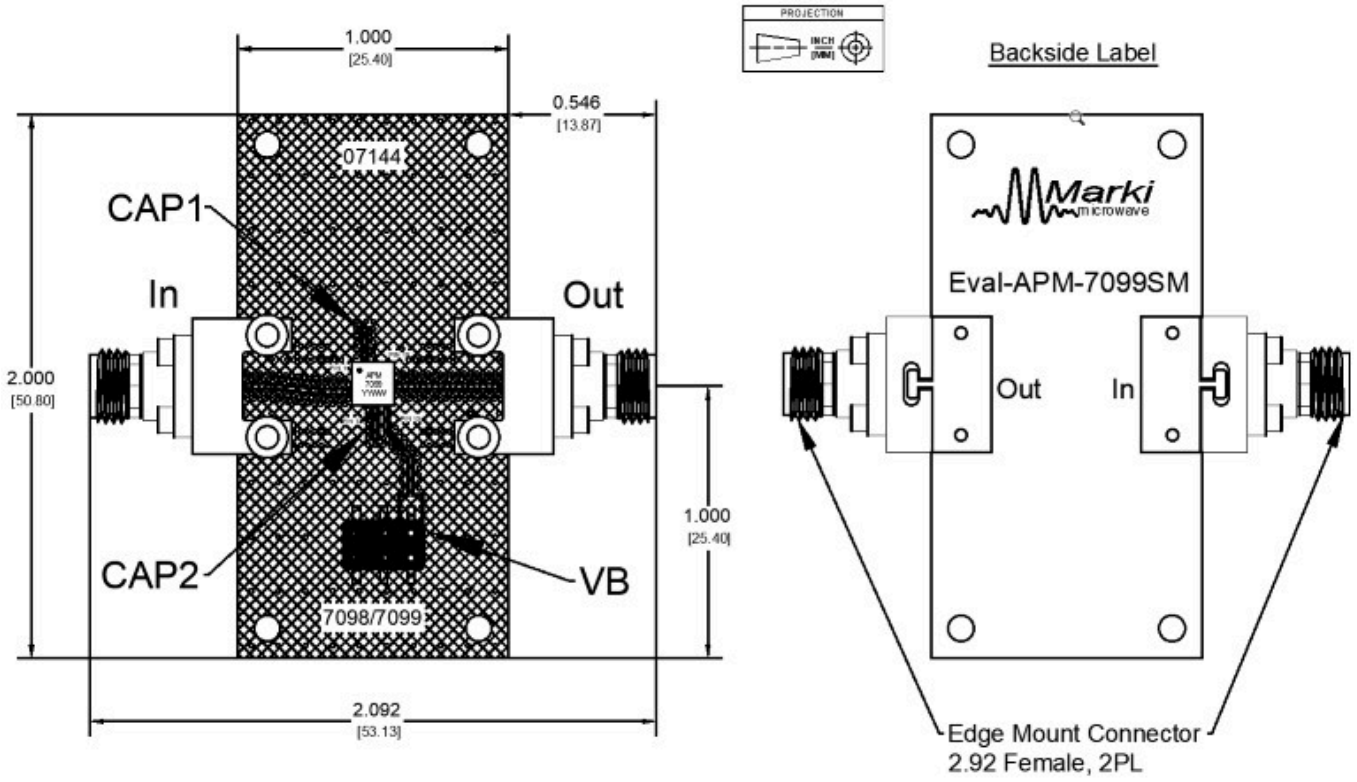
Notes:

1. Substrate Material is Plastic.
2. I/O Leads and Die Paddle are 0.05 microns Au over 0.02 microns Pd over 0.5 microns Ni.
3. All unconnected pins should be connected to PCB RF ground.

Footprint Image



Evaluation Board - Outline Drawing



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