

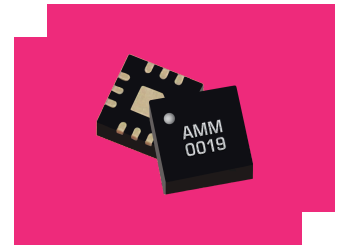
AMM-10861PSM

15-45 GHz Broadband Gain Block Driver Amplifier

DEVICE OVERVIEW

General Description

The AMM-10861PSM is a wideband pHEMT-based GaAs surface-mount gain block driver amplifier operating from 15 to 45 GHz. This amplifier offers high gain at 24 dB, +21 dBm saturated output power, and strong linearity with output IP3 of +28 dBm. It's an excellent driver for our H- and S-diode mixers and multipliers, and comes in a compact 3 mm surface-mount package for easy integration onto printed circuit boards.



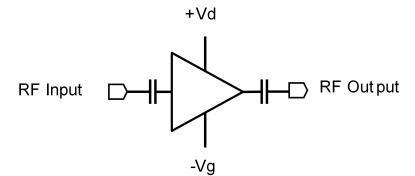
Features

- Wideband, 15 to 45GHz
- High Gain, 24 dB Typical
- High Output Power, +21 dBm Typical
- Minimal Application Circuit
- Internal Blocking Capacitors
- Small 3 x 3 mm QFN Package

Applications

- Electronic Warfare
- Radar
- Satellite Communications
- Driver Amplifier for H and S - Diode Mixers
- Test and Measurement Equipment

Functional Block Diagram



Part Ordering Options

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
AMM-10861PSM	15-45 GHz Broadband Gain Block Driver Amplifier	Plastic QFN	REACH RoHS	Released	3A001.b.2.f
EVB-AMM-10861P	Evaluation Board, 15 - 45 GHz Broadband Power Amplifier	EVB	REACH RoHS	Released	EAR99

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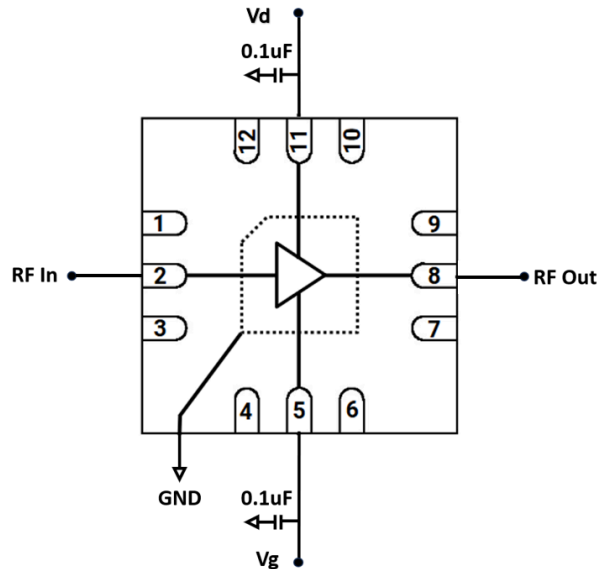
Revision History

Revision Code	Revision Date	Comment
-	2026-04-01	Initial Release

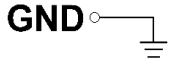
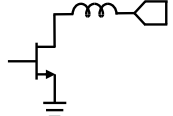
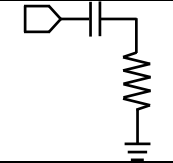
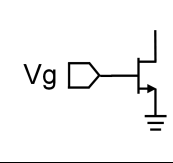
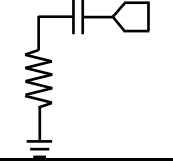
Port Configuration and Functions

Port Diagram

A port diagram of the AMM-10861PSM is shown below (X-ray view).



Port Functions

Port	Function	Description	DC Equivalent Circuit
Ground Paddle	Ground	Ground paddle and non-connected pins must be connected to a DC/RF ground potential with high thermal and electrical conductivity, and low inductance.	GND 
Pin 11	Vd	Pin 11 is the DC bias supply for the amplifier. The voltage at this pin should be set to 4V for normal operation. This part requires an off-chip bypass capacitor of 0.1uF installed at this pin as close to the IC as possible. See applications circuit.	
Pin 2	RF Input	Pin 2 is the amplifier's RF input pin. This port is internally matched to 50 Ohms and is internally DC blocked.	
Pin 5	Vg	This is the negative DC bias voltage for the amplifier IC. The voltage at this pin controls the current draw Id of the part. Higher voltage results in higher current. For normal operation, the voltage at this pin is adjusted to produce an Id of 158mA when Vd=4V. This part requires an off-chip 0.1uF bypass capacitor installed at this pin as close to the IC as possible. See applications circuit.	
Pin 8	RF Output	Pin 8 is the amplifier's RF output pin. This port is internally matched to 50 Ohms and is internally DC blocked. Equivalent circuit for the RF Output	

Specifications

Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If these limits are exceeded, the device may be inoperable or have a reduced lifetime. This amplifier is designed and characterized in a 50Ω system, and operation in a reflective environment can cause performance degradation.

Parameter	Maximum Rating	Unit
Maximum Operating Temperature	85	°C
Maximum Storage Temperature	150	°C
Max Junction Temperature for MTTF > 1E6 hours	175	°C
Minimum Operating Temperature	-40	°C
Minimum Storage Temperature	-65	°C
Positive Drain Supply Current (with RF Input)	200	mA
Positive Drain Supply Voltage (Vd)	4.5	V
RF Input Power	15	dBm
Gate Supply Voltage (Vg)	0	V
Thermal Resistance, θ_{JC}	110	°C/W

Package Information

Parameter	Details	Rating
ESD	< 250 Volts	HBM Class 0
Dimensions	-	3 x 3 mm
Moisture Sensitivity Level	-	MSL 1

Recommended Operating Conditions

The Recommended Operating Conditions indicate the limits, inside which the device should be operated, to guarantee the performance given in Electrical Specifications. Operating outside these limits may not necessarily cause damage to the device, but the performance may degrade outside the limits of the Electrical Specifications. For limits, above which damage may occur, see Absolute Maximum Ratings .

Parameter	Min	Nominal	Max	Unit
Ambient Temperature	-40	25	85	°C
Gate Bias DC Voltage (Vg)	-0.3	-0.16	-0.05	V
Power Supply DC Voltage (Vd)	3	4	4	V
Positive DC Current (Id) (No RF Input)	98	158	190	mA

Sequencing Requirements

Turn-on Procedure:

1. Apply Vg
2. Apply Vd

Turn-off Procedure:

1. Turn off Vd
2. Turn off Vg

Note: RF input power can be injected at any moment in the bias sequencing procedure.

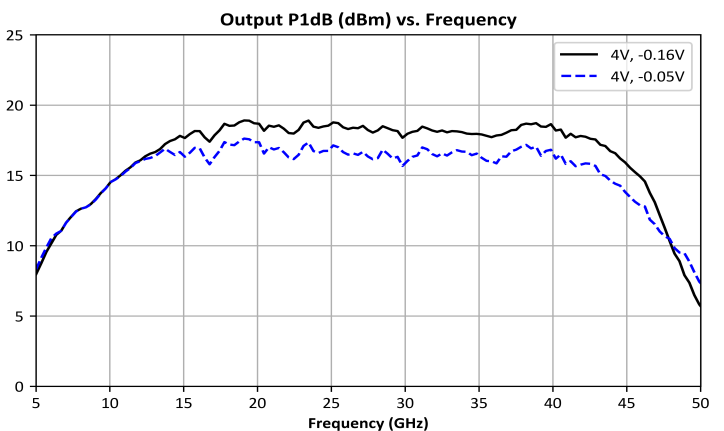
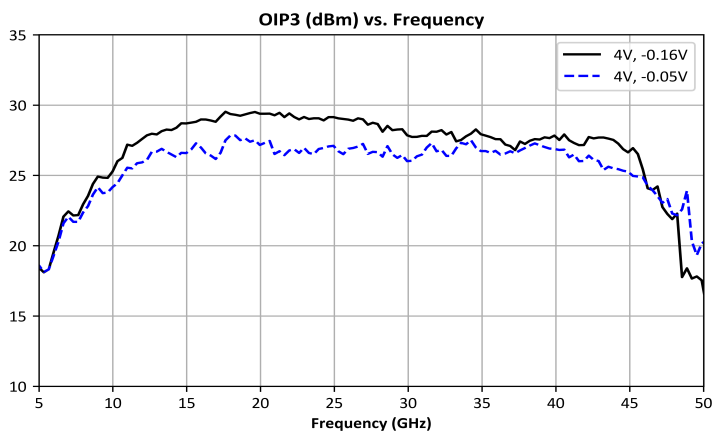
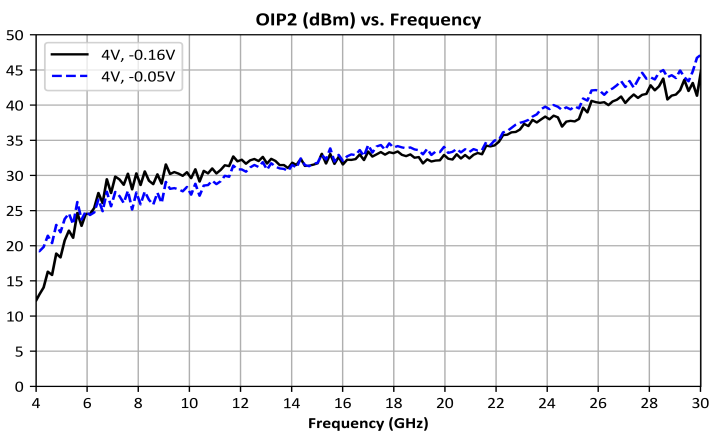
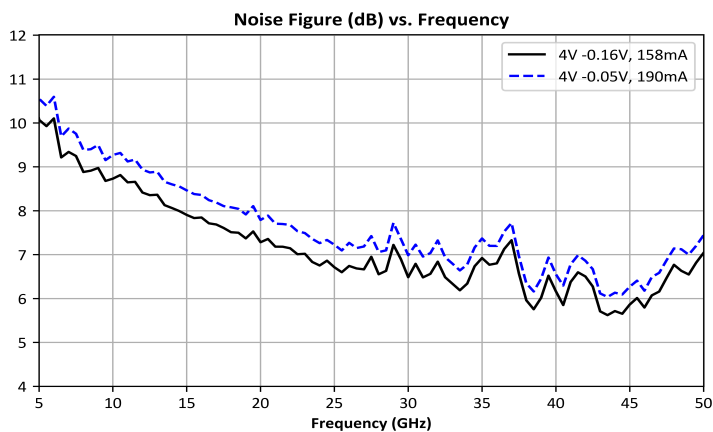
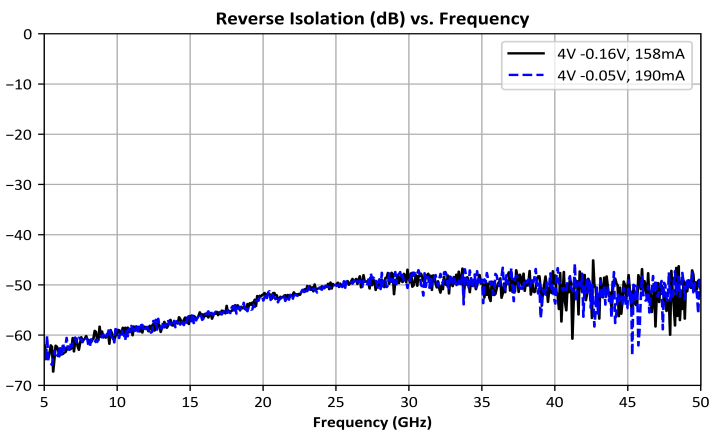
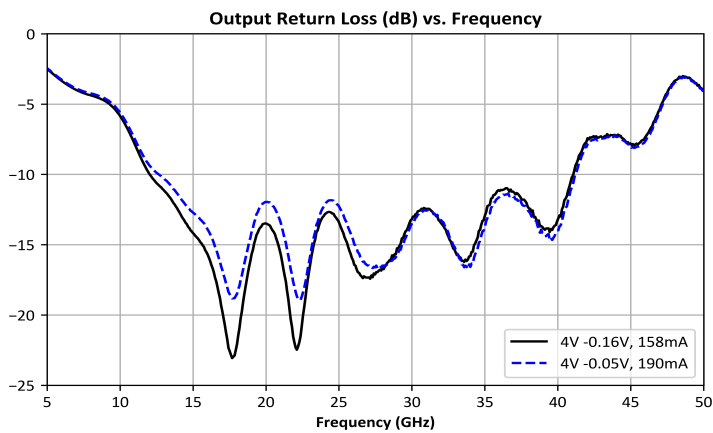
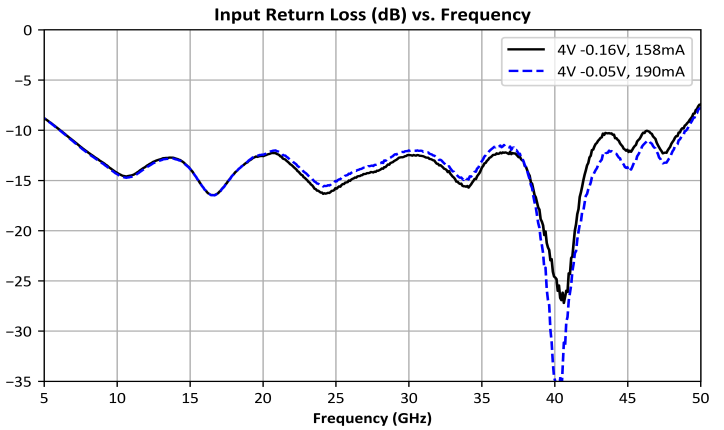
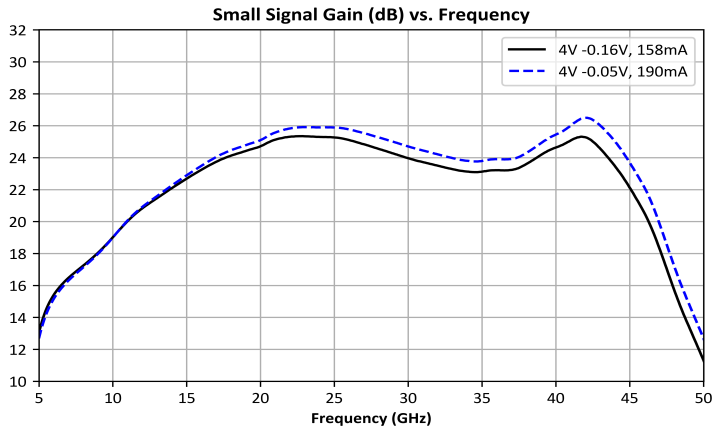
Electrical Specifications

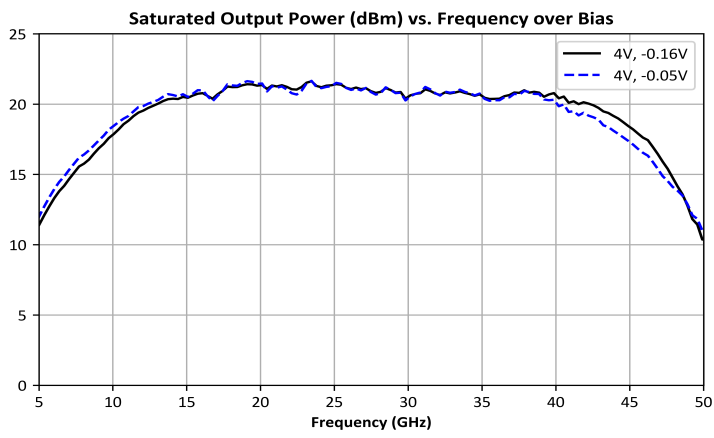
The electrical specifications apply at TA=+25°C in a 50Ω system. QFNs are 100% RF tested.

Parameter	Test Conditions	Minimum Frequency (GHz)	Maximum Frequency (GHz)	Min	Typ	Max	Unit
Small Signal Gain	4V/-0.16V, 158mA	15	45	-	24.2	-	dB
Input Return Loss	4V/-0.16V, 158mA	15	45	-	14	-	dB
Output Return Loss	4V/-0.16V, 158mA	15	45	-	14	-	dB
Reverse Isolation	4V/-0.16V, 158mA	15	45	-	50	-	dB
Saturated Output Power	4V/-0.16V, 158mA	15	45	-	20.82	-	dB
Input P1dB	4V/-0.16V, 158mA	15	45	-	-4.5	-	dBm
Output P1dB	4V/-0.16V, 158mA	15	45	-	18	-	dBm
Input IP3	4V/-0.16V, 158mA, -18dBm input, 1 MHz tone spacing	15	45	-	4	-	dBm
Output IP3	4V/-0.16V, 158mA, -18dBm input, 1 MHz tone spacing	15	45	-	28	-	dBm
Input IP2	4V/-0.16V, 158mA, -20dBm input, 1 MHz tone spacing	15	23	-	8.5	-	dBm
Output IP2	4V/-0.16V, 158mA, -20dBm input, 1 MHz tone spacing	15	23	-	33	-	dBm
Noise Figure	4V/-0.16V, 158mA	15	45	-	6.8	-	dB
Current Consumption ¹	4V/-0.16V	-	-	-	158	-	mA

^[1] Bias conditions for Id tested with no RF input power. Bias conditions presented as Vd/Vg

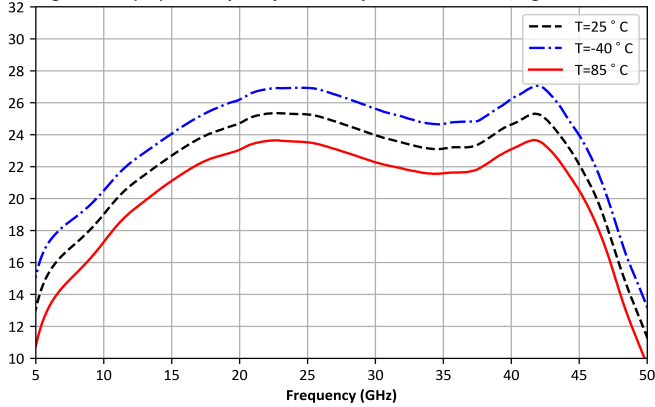
Typical Performance Plots (vs Bias)



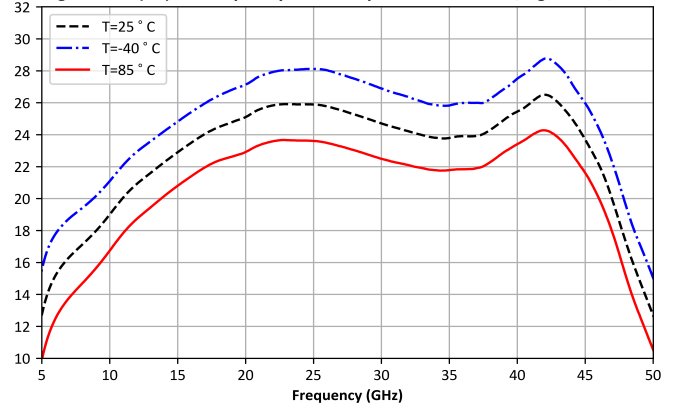


Typical Performance Plots (vs Temperature)

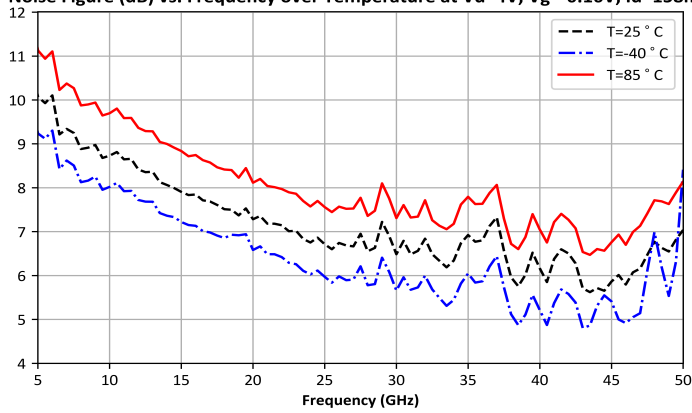
Small Signal Gain (dB) vs. Frequency over Temperature at Vd=4V, Vg=-0.16V, Id=158mA



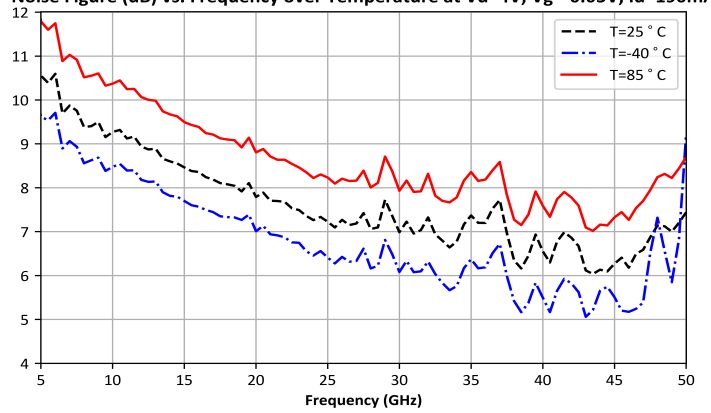
Small Signal Gain (dB) vs. Frequency over Temperature at Vd=4V, Vg=-0.05V, Id=190mA



Noise Figure (dB) vs. Frequency over Temperature at Vd=4V, Vg=-0.16V, Id=158mA



Noise Figure (dB) vs. Frequency over Temperature at Vd=4V, Vg=-0.05V, Id=190mA



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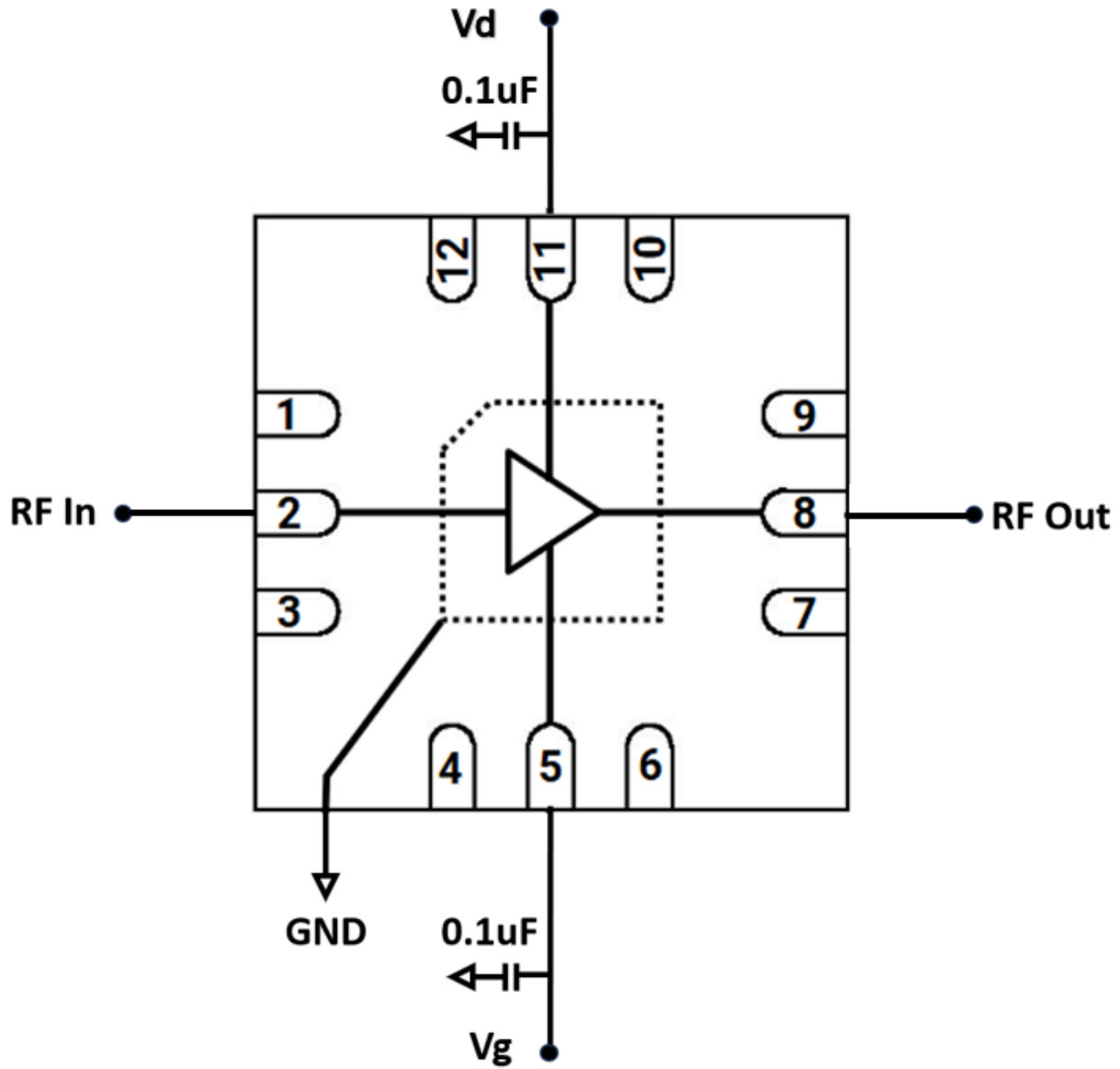
Application Information

Below is the recommended application circuit for the AMM-10861PSM. This is the configuration that is used to characterize this device. However, each PCB layout and environment are different which may require minor modifications of the biasing network. Please contact support@markimicrowave.com for more information.

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15-45 GHz Broadband Gain Block Driver Amplifier

Application Circuit



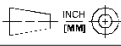
Application Circuit Description

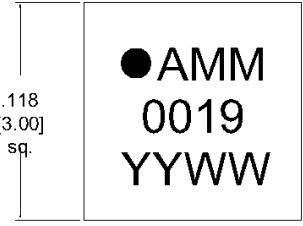
Above is the recommended application circuit for the AMM-10861PSM. DC drain voltage is supplied to the amplifier across a 0.1uF bypass capacitor to the Vd pin. DC gate voltage is supplied to the amplifier across a 0.1uF bypass capacitor to the Vg pin. The RF input and output ports are internally DC blocked.

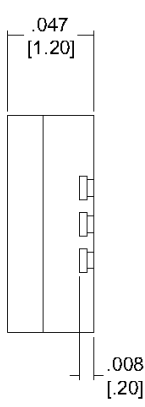
Mechanical Data

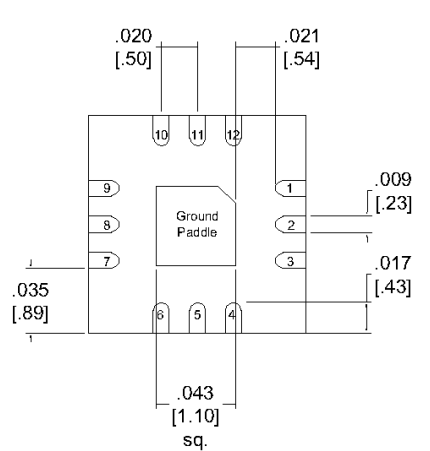
Outline Drawing

Download : [Outline 2D Drawing](#) | [Outline 3D Drawing](#) | [Outline 3D STP](#)

PROJECTION		REVISIONS			
	INCH [MM]	REV.	DESCRIPTION	DATE	APPROVALS
		A	Initial Release	2/24/26	AT








Pin #	Function
1	GND
2	RF In
3	GND
4	GND
5	Vg
6	GND
7	GND
8	RF Out
9	GND
10	GND
11	Vd
12	GND

Notes (unless otherwise specified):

- Substrate material is LCP.
- I/O Leads and Die Paddle is (from base to finish):
 Ni: 0.5 - 2.0um
 Pd: 0.08 - 0.15um
 Au: 0.008 - 0.05um
- All unconnected pins should be connected to PCB RF ground.

J:\L253\OT\15-45 GHz Broadband Gain Block Driver Amplifier\AMM-10861PSM\15-45 GHz Broadband Gain Block Driver Amplifier\AMM-10861PSM.dwg 11/19/2025 AD 11/19/2025	NOTES: 1. ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED. 2. DIMENSIONS ARE TO CENTER UNLESS OTHERWISE SPECIFIED. 3. DIMENSIONS ARE TO CENTER UNLESS OTHERWISE SPECIFIED. 4. DIMENSIONS ARE TO CENTER UNLESS OTHERWISE SPECIFIED. 5. DIMENSIONS ARE TO CENTER UNLESS OTHERWISE SPECIFIED.	 Outline 3mm QFN Amplifier DWG. NO. AMM-10861PSM
MATERIAL: 220-10861A FINISH: As Noted	DRAWN BY: AD DATE: 11/19/2025 AN, AC 1/15/2026	SIZE: A CAGE CODE: 0UC32 SHEET 1 OF 1

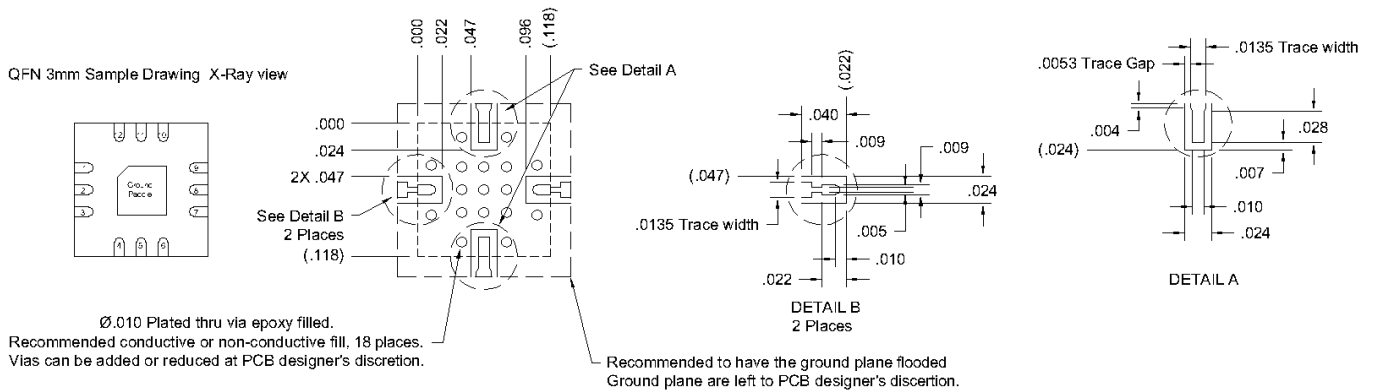
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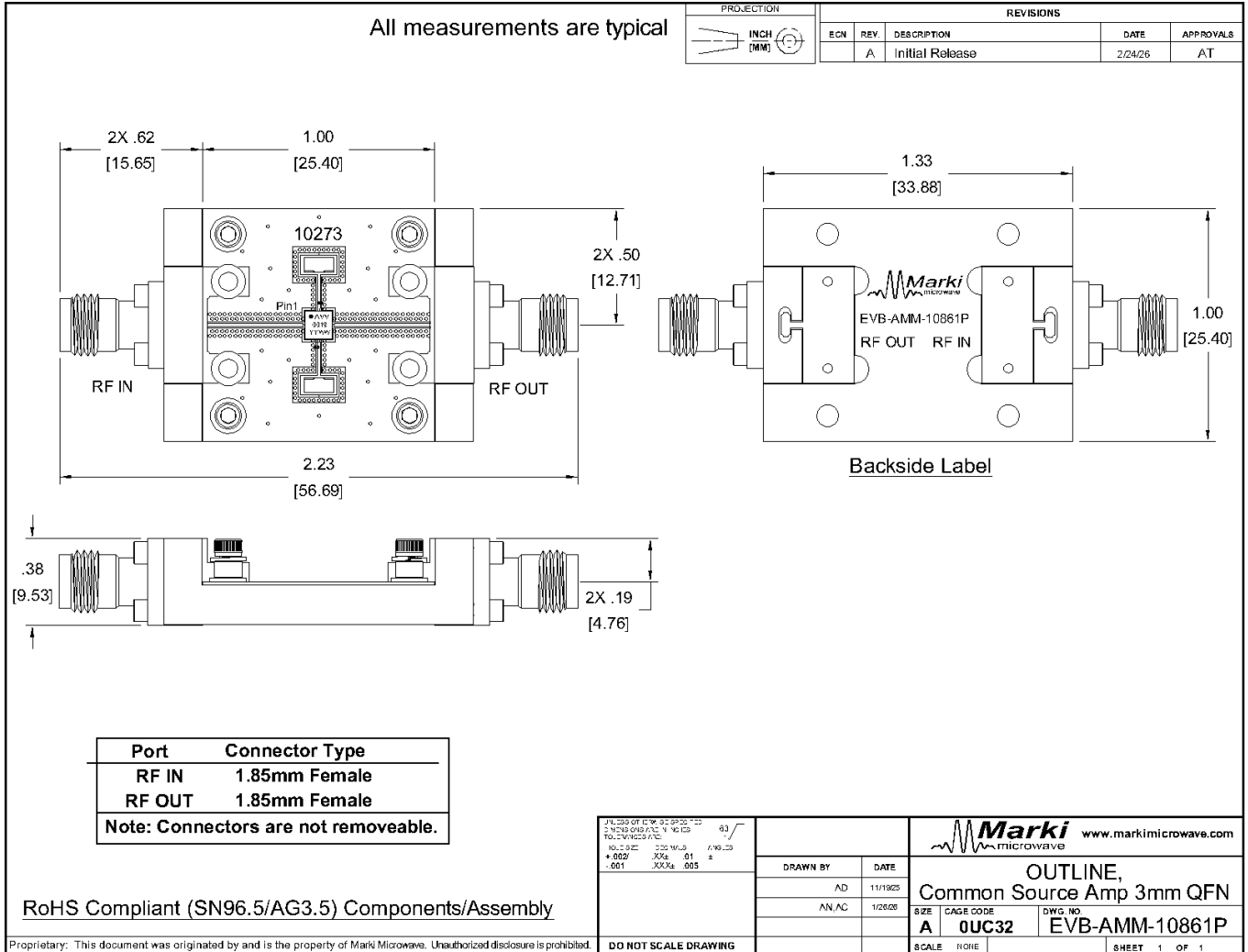
Footprint Image

Download : [Footprint Drawing](#)



The landing pattern is to be used on Rogers 4003,
0.008" thick, ½ Oz Cu.

Evaluation Board - Outline Drawing



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