Sales: 408-778-9952 | General: 408-778-4200 | Fax: 408-778-4300
Sales & Customer Support: sales@markimicrowave.com
Tech Support: support@markimicrowave.com

ADM-8096CH

0.09 - 6 GHz High Dynamic Range Gain Block

DEVICE OVERVIEW

General Description

The ADM-8096CH is a high-linearity low noise amplifier capable of providing +23 dBm output power up to 6 GHz. The ADM-8096CH can serve either as a linear signal amplifier, or as a saturated driver amplifier for H- or S-diode mixers. The amplifier has excellent return losses and gain flatness.

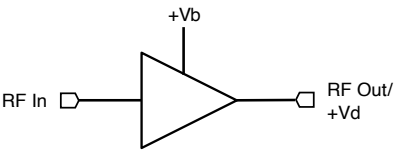
Features

- +23 dBm output power
- +22 dB gain
- 1.5 dB noise figure
- Excellent Gain flatness
- No negative bias required

Applications

- Mobile test and measurement equipment
- Radar and satellite communications
- 5G transceivers
- Driver Amplifier for H and S - Diode Mixers

Functional Block Diagram



Part Ordering Options

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
ADM-8096CH	0.09 - 6 GHz High Dynamic Range Gain Block	CH	REACH RoHS	Released	EAR99

Table Of Contents

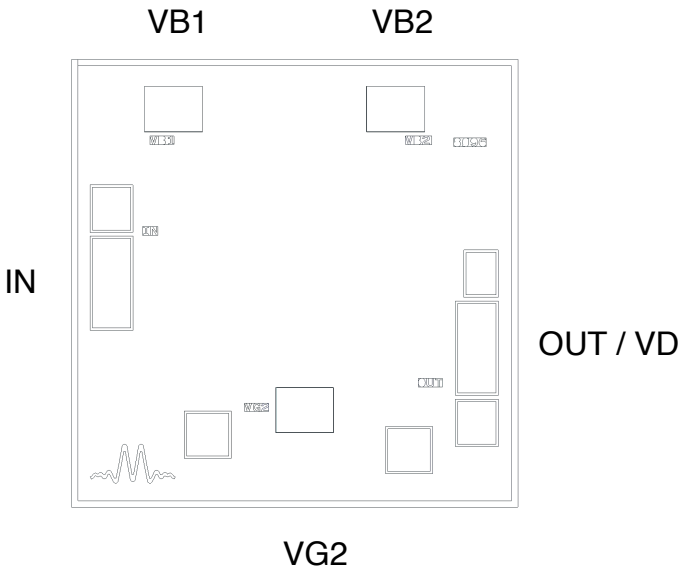
Revision History

Revision Code	Revision Date	Comment
-	2023-12-13	Initial Release

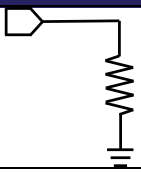
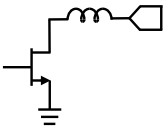
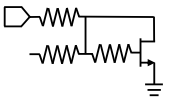
Port Configuration and Functions

Port Diagram

A port diagram of the ADM-8096CH bare die is shown below.



Port Functions

Port	Function	Description	Equivalent Circuit for Package
IN	RF Input	This is the RF Input port of the amplifier. It is internally RF matched to 50 Ω and requires an external DC blocking cap.	
OUT	Drain Supply / RF Output	This is the RF Output port and is also the Vd port providing the main power supply to the amplifier. This pin is DC coupled and requires an external bias-T or discrete choke and DC blocking capacitor. This port is RF matched to 50 Ω. DC voltage at this pin should be set to 5V for normal operation.	
Paddle	Gnd	Ground is provided through the backside of the die. See mounting instructions for more information on mounting practices for best thermal and electrical performance.	-
VB1	Non-connect (NC)	Do not connect this pad.	-
VB2	Vb	This pad provides DC bias to the amplifier. Placement of an external series bias resistor allows this pin to be supplied by the same supply line providing 5V to the RF Out/Vd pad. For normal operation, this pad can be left floating. DO NOT GROUND this pad. Device drain current will change proportional to the current flowing into this pin. RF performance can be balanced with DC power consumption by adjusting the current into this pin.	
VG2	Non-connect (NC)	Do not connect this pad.	-

Specifications

Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If any one of these limits are exceeded, the device may become inoperable or have a reduced lifetime. Reliability limits are individual, instantaneous catastrophic limits only. Functional operation limits are indicated below. Operation of the device at multiple absolute maximum limits or for extended periods at a single limit can cause degradation and damage to the device.

Parameter	Maximum Rating	Unit
Bias Voltage (Vb)	8	V
Drain Current (No RF Applied)	222	mA
Drain Supply Voltage (Vd)	8	V
Maximum Operating Temperature for MTTF > 1E6 hours	85	°C
Maximum Storage Temperature	125	°C
Max Junction Temperature for MTTF of 1E6 hours	175	°C
Max Power Dissipation for MTTF of 1E6 hours	0.72	W
Minimum Operating Temperature for MTTF > 1E6 hours	-40	°C
Minimum Storage Temperature	-65	°C
RF Input Power	15	dBm
θ_Jc, Junction to Case Thermal Resistance	65	°C/W

Package Information

Parameter	Details	Rating
Dimensions	-	1.05 x 1.05 mm

Recommended Operating Conditions

The Recommended Operating Conditions indicate the limits, inside which the device should be operated, to guarantee the performance given in Electrical Specifications Operating outside these limits may not necessarily cause damage to the device, but the performance may degrade outside the limits of the electrical specifications. For limits, above which damage may occur, see Absolute Maximum Ratings.

Parameter	Min	Nominal	Max	Unit
Ambient Temperature	-40	25	85	°C
Power Supply DC Voltage (Vd)	3	5	6	V
Input Power for Saturation	2	4	6	dBm
Power Supply DC Current (Id) (No RF Input) [1]	31	58	71	mA

[1] Recommended operating current conditions without RF input applied.

Sequencing Requirements

There is no sequencing required to power up or power down the amplifier. The amplifier must have an output load connected during operation.

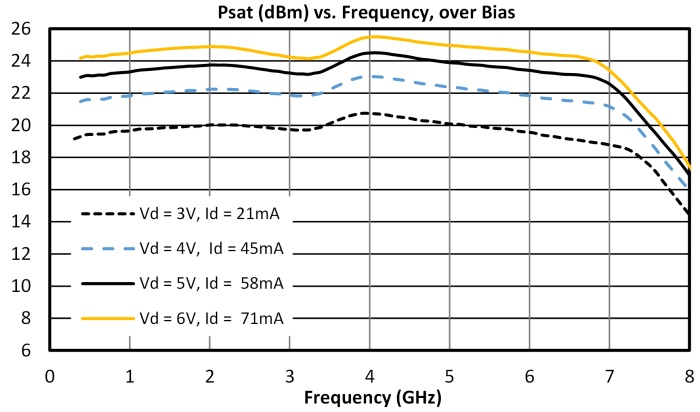
Electrical Specifications

Unless otherwise specified, electrical specifications apply at TA=+25°C, Vd = 5V and Vb = Float.

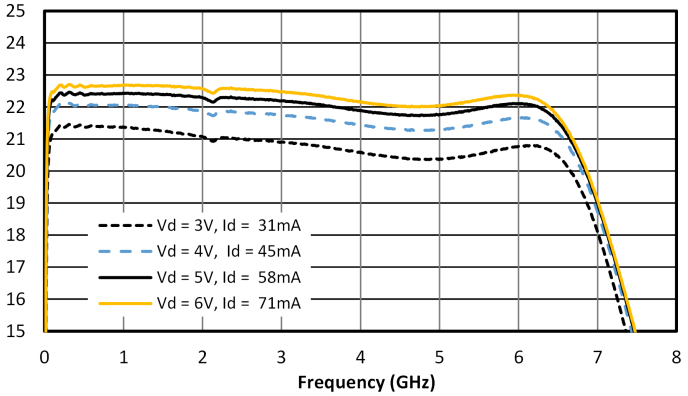
Parameter	Test Conditions	Minimum Frequency (GHz)	Maximum Frequency (GHz)	Min	Typ	Max	Unit
DC Supply Quiescent Current (Idq)	Vd = 5 V, no RF input	-	-	-	58	-	mA
Input IP3	Vd = 5 V, Pin = -15 dBm per tone, 10 MHz tone spacing	0.09	6	-	11	-	dBm
Input Power for Saturation	Vd = 5V	0.09	6	-	4	-	dBm
Input Return Loss	Vd = 5 V, Pin = -20 dBm	0.09	6	-	15	-	dB
Noise Figure	Vd = 5 V, Pin = -20 dBm	3	6	-	1.9	-	dB
Noise Figure	Vd = 5 V, Pin = -20 dBm	0.09	3	-	1.5	-	dB
Output IP2	Vd = 5 V, Pin = -15 dBm per tone, 10 MHz tone spacing	0.09	6	-	35	-	dBm
Output IP3	Vd = 5 V, Pin = -15 dBm per tone, 10 MHz tone spacing	0.09	6	-	33	-	dBm
Output P1dB	Vd = 5V	0.09	6	-	21	-	dBm
Output Power	Vd = 5 V	0.09	6	-	23	-	dBm
Output Return Loss	Vd = 5 V, Pin = -20 dBm	0.09	6	-	17	-	dB
Reverse Isolation	Vd = 5 V, Pin = -20 dBm	0.09	6	-	28	-	dB
Small Signal Gain	Vd = 5 V, Pin = -20 dBm	0.09	6	-	22	-	dB

Typical Performance Plots

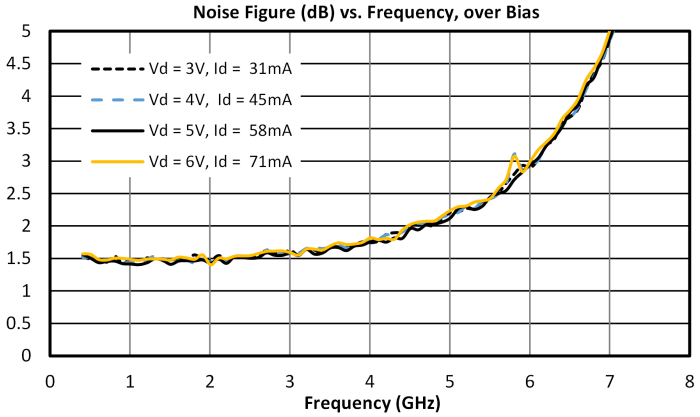
Psat (dBm) vs. Frequency, over Bias



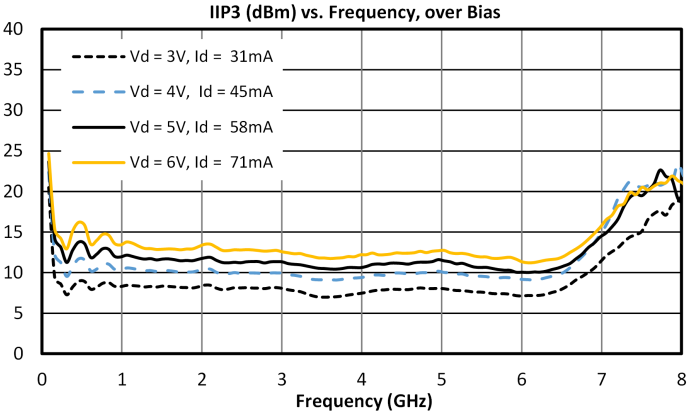
Small Signal Gain (dB) vs. Frequency, over Bias



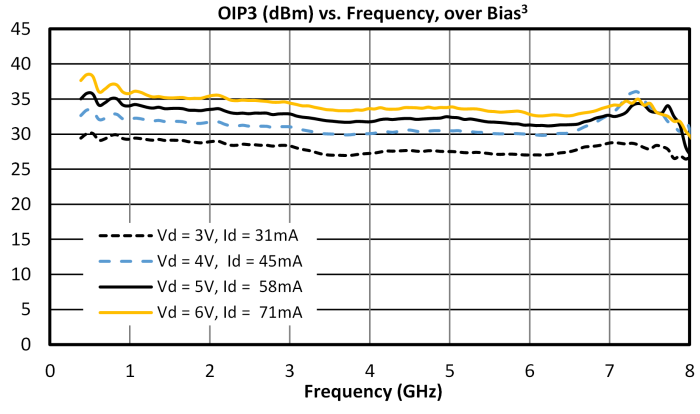
Noise Figure (dB) vs. Frequency, over Bias



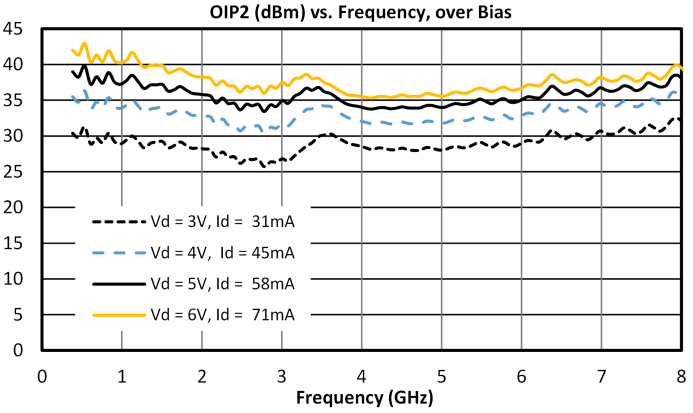
IIP3 (dBm) vs. Frequency, over Bias



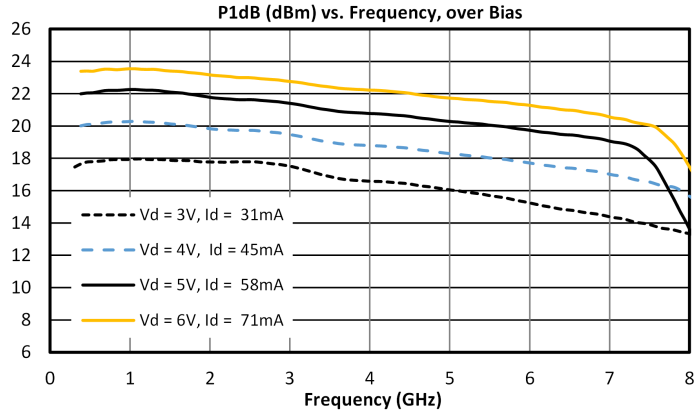
OIP3 (dBm) vs. Frequency, over Bias[3]



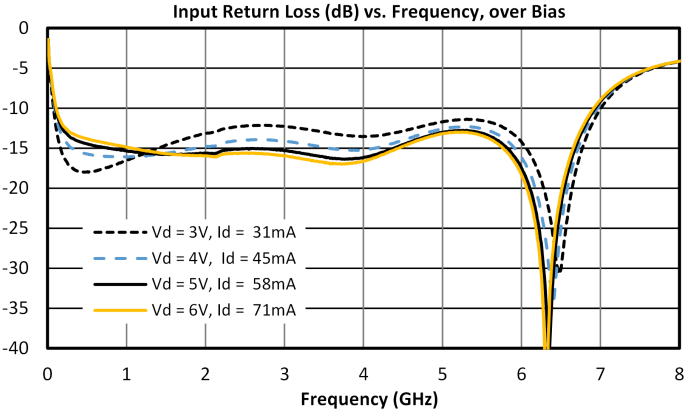
OIP2 (dBm) vs. Frequency, over Bias



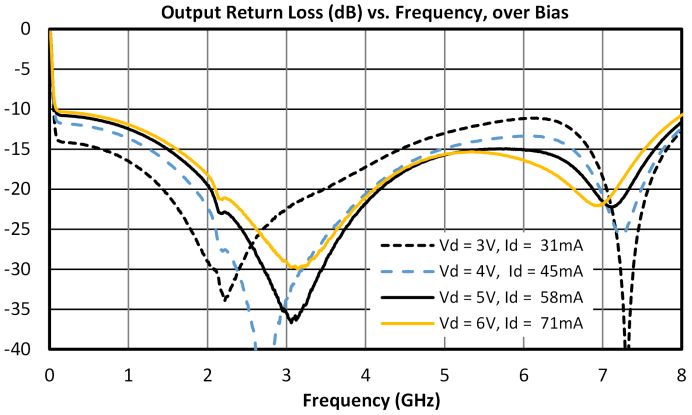
P1dB (dBm) vs. Frequency, over Bias



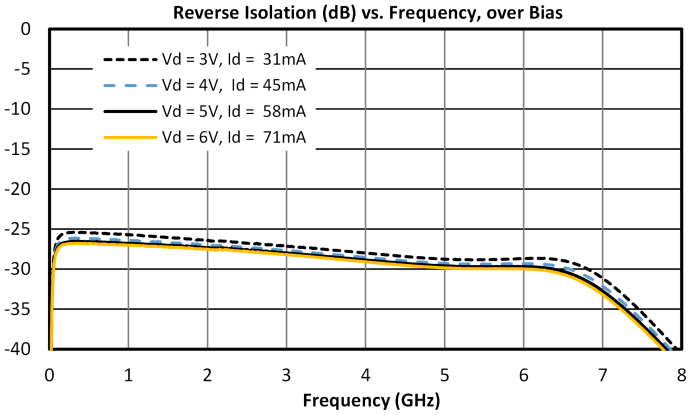
Input Return Loss (dB) vs. Frequency, over Bias



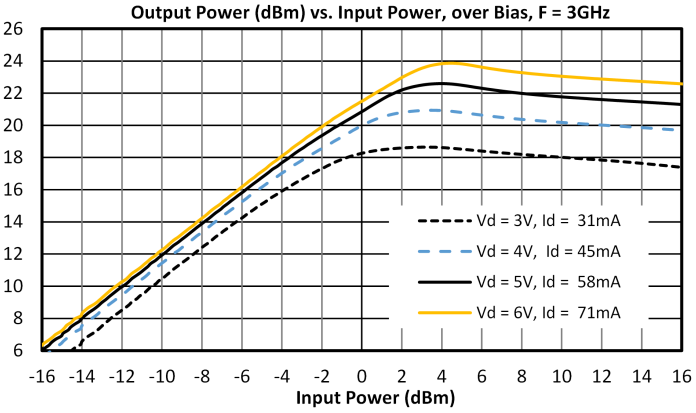
Output Return Loss (dB) vs. Frequency, over Bias



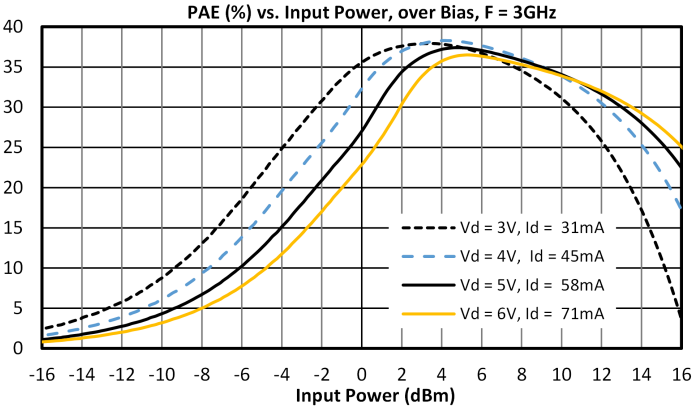
Reverse Isolation (dB) vs. Frequency, over Bias



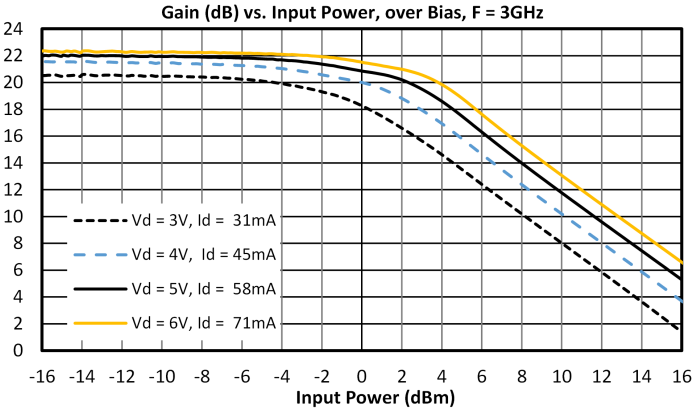
Output Power (dBm) vs. Input Power, over Bias, F = 3GHz



PAE (%) vs. Input Power, over Bias, F = 3GHz



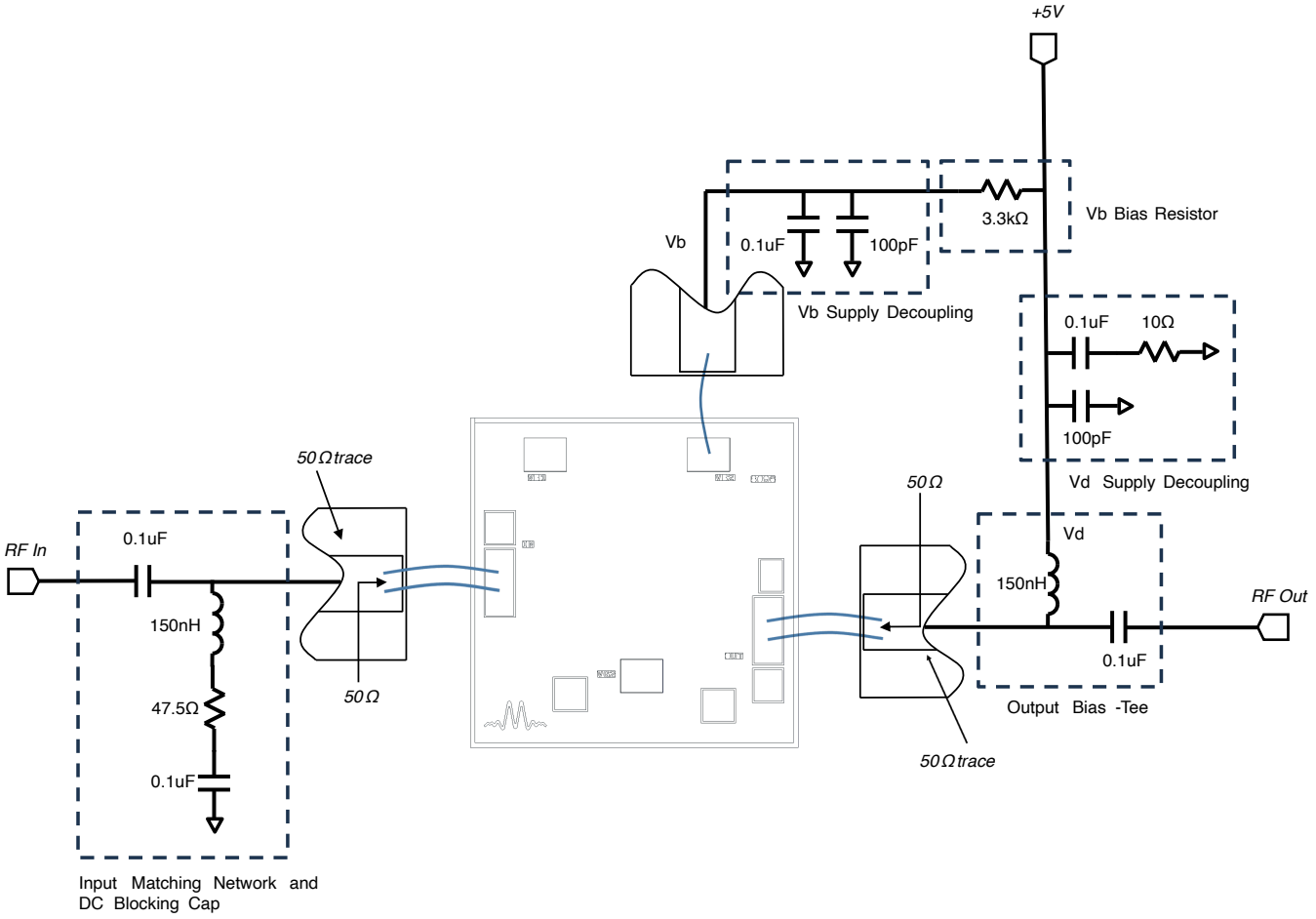
Gain (dB) vs. Input Power, over Bias, F = 3GHz



Application Information

Below is the recommended application circuit for the ADM-8096CH. DC power is supplied to RF Out/Vd pad via a 150 nH choke inductor. Supply bypassing is provided by 100pf and 0.1uF capacitors. Drain current Id can be controlled by applying voltage to VB2 pad. Drain current Id is adjusted proportionally to the current flowing into the VB2 pad with higher Vb and Ib resulting in increased current Id. Amplifier performance can therefore be optimized for specific applications by adjusting the value of series resistor Rb on the Vb line. In particular, OIP3 across the band and especially at low frequencies can be improved from that shown in the electrical specs table by increasing current into VB2. The OIP3 can be improved by up to 5dB with the tradeoff being increased quiescent DC power consumption. The application schematic shows a resistor in series on the Vb line; However, the default configuration is to leave this resistor un-populated and leave the VB2 pad un-connected or floating. The ADM-8096CH requires an RF input matching network at the RF In pad as shown. DC blocking capacitors are also required at RF input and output pins as shown. VB1 and VG2 pads should be left floating and un-connected. Contact support@markimicrowave.com if you would like help creating an alternative application circuit for your system's requirements.

Application Circuit



Die Mounting Recommendations

Mounting and Bonding Recommendations

Marki MMICs should be attached directly to a ground plane with conductive epoxy. The ground plane electrical impedance should be as low as practically possible. This willprevent resonances and permit the best possible electrical performance. Datasheetperformance is only guaranteed in an environment with a low electrical impedance ground.

Mounting - To epoxy the chip, apply a minimum amount of conductive epoxy to themounting surface so that a thin epoxy fillet is observed around the perimeter of the chip.Cure epoxy according to manufacturer instructions.

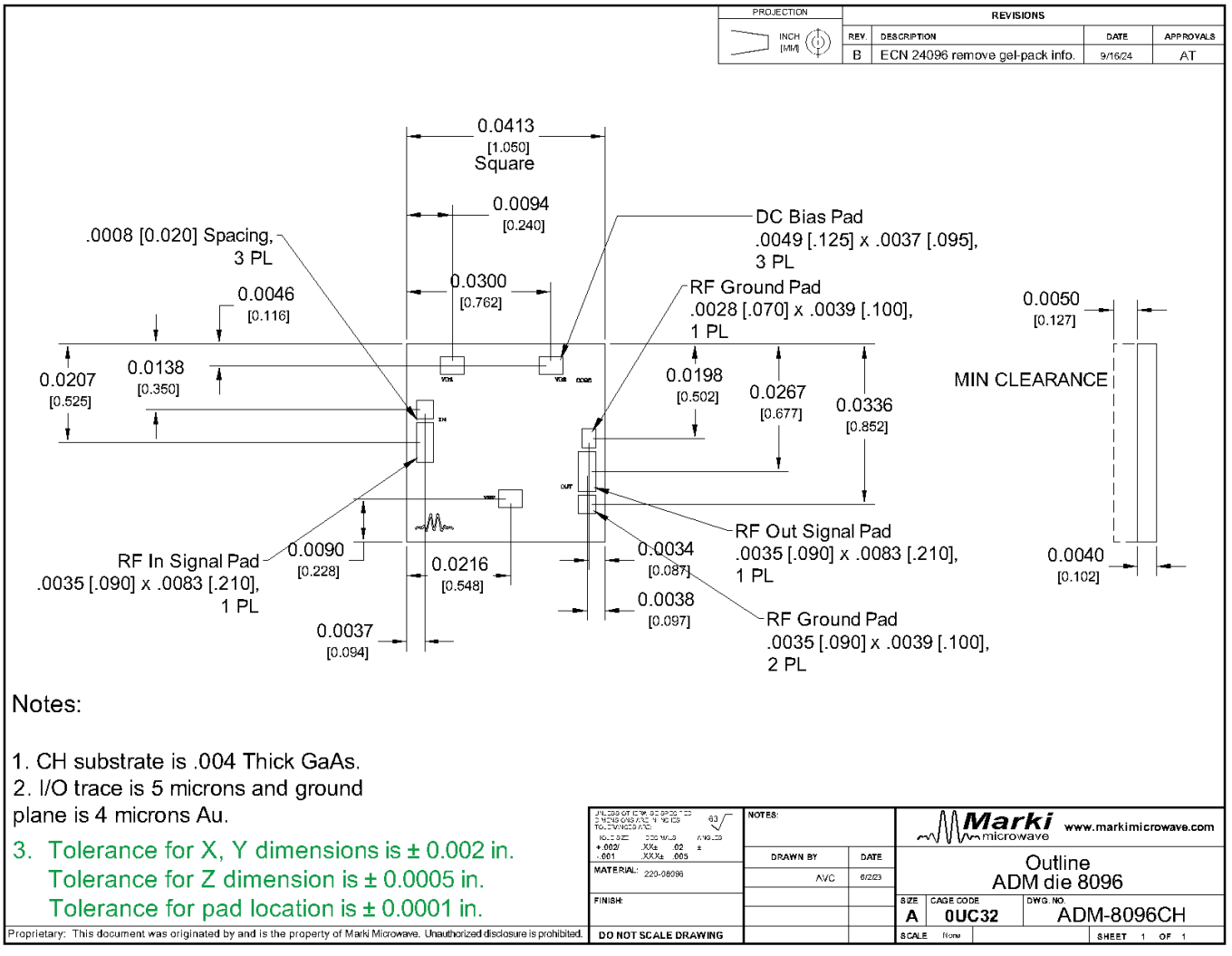
Wire Bonding - Ball or wedge bond with 0.025 mm (1 mil) diameter pure gold wire.Thermosonic wirebonding with a nominal stage temperature of 150 °C and a ball bondingforce of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Usethe minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should bestarted on the chip and terminated on the package or substrate. Bond wire inductancewill improve return loss. Bondwire inductance in the range of 30pH to 200pH will improveperformance.

Circuit Considerations – 50 Ω transmission lines should be used for all high frequencyconnections in and out of the chip. Wirebonds should be kept as short as possible, withmultiple wirebonds recommended for higher frequency connections to reduce parasiticinductance. In circumstances where the chip more than .001” thinner than thesubstrate, a heat spreading spacer tab is optional to further reduce bondwire length and parasitic inductance.

Mechanical Data

Outline Drawing

Download : Outline 2D Drawing



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