

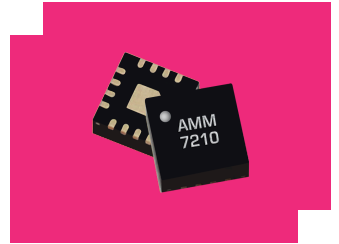
AMM-7210SM

25-50 GHz GaAs Surface Mount LO Driver Amplifier

DEVICE OVERVIEW

General Description

The AMM-7210SM is a surface-mount amplifier suitable for use as a single tone driver or general-purpose gain block. It can drive an L or H diode mixer from 25 to 50 GHz, or S diode mixer from 27 to 50 GHz. This amplifier also has exceptionally low input and output reflections, and a positive gain slope. The AMM-7210SM is packaged in a compact 3mm QFN for surface mount integration onto printed circuit boards.



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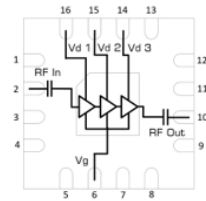
Features

- +15 dB Small Signal Gain
- +23 dBm saturated output power
- Excellent return losses
- Compact 3mm QFN package

Applications

- Radar and satellite communications
- 5G transceivers
- LO Driver amplifier for L-, H-, or S-diode mixers
- Mobile test and measurement equipment

Functional Block Diagram



Part Ordering Options

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification	Recommended Replacement
AMM-7210SM	25-50 GHz GaAs Surface Mount LO Driver Amplifier	QFN	REACH RoHS	End of Life	3A001.b.2.d	AMM-8211PSM
EVAL-AMM-7210SM	25-50 GHz GaAs Surface Mount LO Driver Amplifier	EVAL	REACH RoHS	End of Life	EAR99	EVB-AMM-8211P

AMM-7210SM

25-50 GHz GaAs Surface Mount LO Driver Amplifier

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Revision History

Revision Code	Revision Date	Comment
-	2021-06-01	Datasheet Initial Release
A	2026-03-19	End of Life

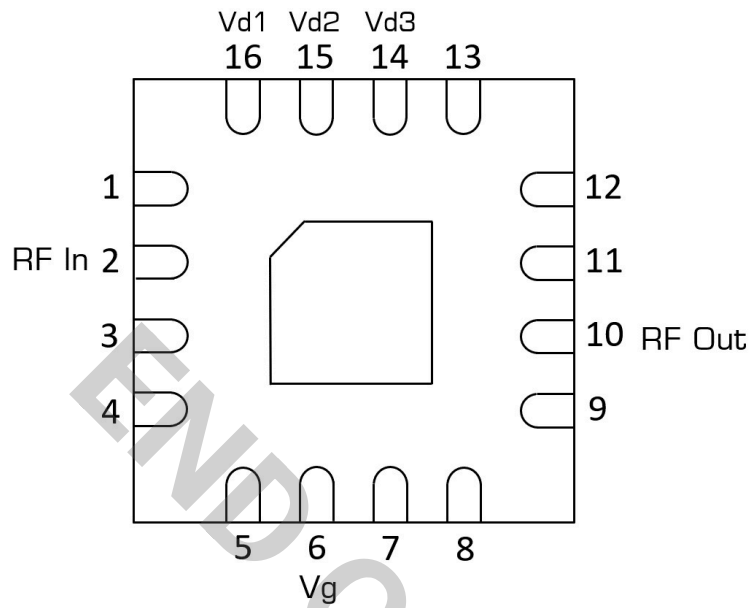
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
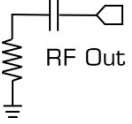
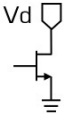
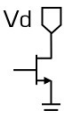
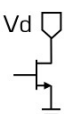
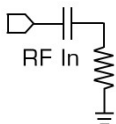
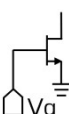
Port Configuration and Functions

Port Diagram

A port diagram of the AMM-7210SM's QFN package is shown below. The pin functions are detailed below.



Port Functions

Port	Function	Description	DC Equivalent Circuit
GND	Ground	Ground paddle and non-connected pins must be connected to a DC/RF ground potential with high thermal and electrical conductivity, and low inductance.	GND 
Pin 10	RF Output	Pin 10 is the RF output of the amplifier, and is matched to 50 ohms. It is internally DC blocked.	 RF Out
Pin 14	Positive DC Supply Vd	Pins 14 provides +2.5V to +4V DC voltage to the amplifier's third stage. Negative voltage must be supplied to Pin 6 before turning on the positive supply voltage.	 Vd
Pin 15	Positive DC Supply Vd	Pins 15 provides +2.5V to +4V DC voltage to the amplifier's second stage. Negative voltage must be supplied to Pin 6 before turning on the positive supply voltage.	 Vd
Pin 16	Positive DC Supply Vd	Pins 16 provides +2.5V to +4V DC voltage to the amplifier's first stage. Negative voltage must be supplied to Pin 6 before turning on the positive supply voltage.	 Vd
Pin 2	RF Input	Pin 2 is the RF input of the amplifier, and is matched to 50 ohms. It is internally DC blocked.	 RF In
Pin 6	Negative DC Supply Vg	Pin 6 provides -0.4V to -0.6V of DC voltage. This must be turned on before turning on the positive supply voltage to Pin 1.	 Vg

Specifications

Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If these limits are exceeded, the device may be inoperable or have a reduced lifetime. This amplifier is designed and characterized in a 50Ω system, and operation in a reflective environment can cause performance degradation. Evaluation board losses are mathematically extracted from Saturated output power, Small signal gain, Noise figure, and IIP3/OIP3 specifications.

Parameter	Maximum Rating	Unit
Continuous Power Dissipation (PDISS) (at 85 °C case temp.) ¹	1	W
Maximum Operating Temperature	85	°C
Maximum Storage Temperature	150	°C
Max Junction Temperature for MTTF > 1E6 Hours	175	°C
Minimum Operating Temperature	-40	°C
Minimum Storage Temperature	-65	°C
Negative Bias Voltage (Pin 6)	-2	V
Positive Drain Supply Current (with RF Input) ²	450	mA
Positive Drain Supply Voltage (Pin 14)	4.5	V
Positive Drain Supply Voltage (Pin 15)	4.5	V
Positive Drain Supply Voltage (Pin 16)	4.5	V
RF Input Power	20	dBm
Thermal Resistance, θJC	94	°C/W

[1] Derates by 11 mW/ °C above 85 °C case temperature.

[2] Positive Drain Supply DC current is specified as Id1 + Id2 + Id3

Package Information

Parameter	Details	Rating
Dimensions	-	3 x 3 mm
Moisture Sensitivity Level	-	MSL 1

Recommended Operating Conditions

The Recommended Operating Conditions indicate the limits, inside which the device should be operated, to guarantee the performance given in Electrical Specifications. Operating outside these limits may not necessarily cause damage to the device, but the performance may degrade outside the limits of the Electrical Specifications. For limits, above which damage may occur, see Absolute Maximum Ratings.

Parameter	Min	Nominal	Max	Unit
Ambient Temperature	-40	25	85	°C
Power Supply DC Voltage Vd1	2.5	3	4	V
Power Supply DC Voltage Vd2	2.5	3	4	V
Power Supply DC Voltage Vd3	2.5	3	4	V
Power Supply DC Current (no RF Input) ¹	115	180	300	mA
Gate Bias DC Voltage	-0.6	-0.5	-0.4	V
Input Power for Saturation	8	11	13	dBm

[1] Power Supply DC current is specified as Id1 + Id2 + Id3

Sequencing Requirements

Turn-on Procedure:

1. Apply Vg (Pin 6)
2. Apply Vd (Pin 14, 15, 16)

Turn-off Procedure:

1. Turn off Vd (Pin 14, 15, 16)
2. Turn off Vg (Pin 6)

Note: RF input power can be injected at any moment in the bias sequencing procedure.

Electrical Specifications

The electrical specifications apply at TA=+25°C in a 50Ω system. QFNs are 100% RF tested. Evaluation board losses are mathematically extracted from Saturated output power, Small signal gain, Noise figure, and IIP3/OIP3 specifications.

Parameter	Test Conditions	Minimum Frequency (GHz)	Maximum Frequency (GHz)	Min	Typ	Max	Unit
Current Consumption ¹	Vd1 = Vd2 = +3V, Vd3 = +3.5V, Vg = -0.4V	-	-	-	230	-	mA
Current Consumption ²	Vd1 = Vd2 = +3V, Vd3 = +3.5V, Vg = -0.5V	-	-	-	180	-	mA
Current Consumption ³	Vd1 = Vd2 = +3V, Vd3 = +3.5V, Vg = -0.6V	-	-	-	130	-	mA
Input IP3	Vd1 = Vd2 = +3V, Vd3 = +3.5V, Vg = -0.5V Bias	25	50	-	11	-	dBm
Input Power for Saturation	Vd1 = Vd2 = +3V, Vd3 = +3.5V, Vg = -0.5V Bias	25	50	-	11	-	dBm
Input Return Loss	Vd1 = Vd2 = +3V, Vd3 = +3.5V, Vg = -0.5V Bias, -20 dBm Input Power	25	50	-	14	-	dB
Noise Figure	Vd1 = Vd2 = +3V, Vd3 = +3.5V, Vg = -0.5V Bias	25	50	-	5.6	-	dB
Output IP3	Vd1 = Vd2 = +3V, Vd3 = +3.5V, Vg = -0.5V Bias	25	50	-	26	-	dBm
Output P1dB	Vd1 = Vd2 = +3V, Vd3 = +3.5V, Vg = -0.5V Bias	25	50	-	20	-	dBm
Output Return Loss	Vd1 = Vd2 = +3V, Vd3 = +3.5V, Vg = -0.5V Bias, -20 dBm Input Power	25	50	-	16	-	dB
Reverse Isolation	Vd1 = Vd2 = +3V, Vd3 = +3.5V, Vg = -0.5V Bias, -20 dBm Input Power	25	50	-	49	-	dB
Saturated Output Power ⁴	Vd1 = Vd2 = +3V, Vd3 = +3.5V, Vg = -0.5V Bias	35	45	17	23	-	dBm
Saturated Output Power ⁵	Vd1 = Vd2 = +3V, Vd3 = +3.5V, Vg = -0.5V Bias	45	50	-	21	-	dBm
Saturated Output Power ⁶	Vd1 = Vd2 = +3V, Vd3 = +3.5V, Vg = -0.5V Bias	25	35	-	20	-	dBm
Small Signal Gain	Vd1 = Vd2 = +3V, Vd3 = +3.5V, Vg = -0.5V Bias, -20 dBm Input Power	35	45	9	15	-	dB
Small Signal Gain	Vd1 = Vd2 = +3V, Vd3 = +3.5V, Vg = -0.5V Bias, -20 dBm Input Power	25	35	-	13	-	dB
Small Signal Gain	Vd1 = Vd2 = +3V, Vd3 = +3.5V, Vg = -0.5V Bias, -20 dBm Input Power	45	50	-	15	-	dB

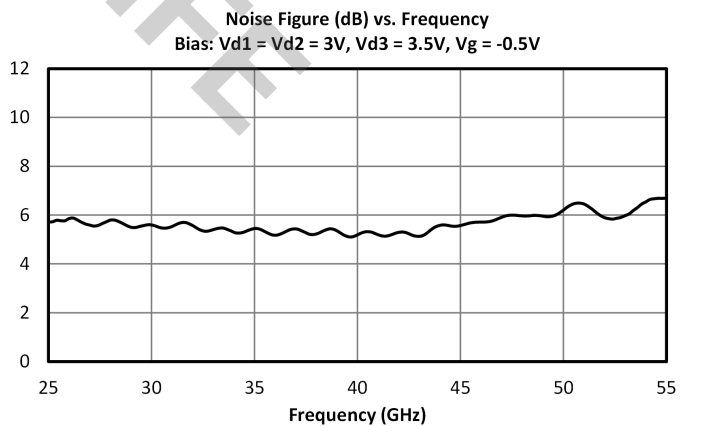
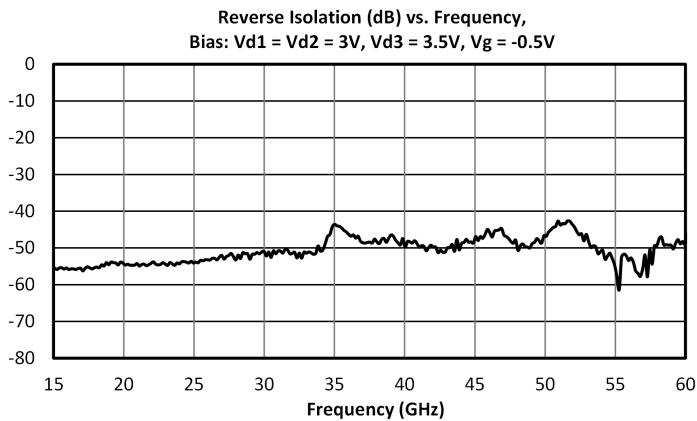
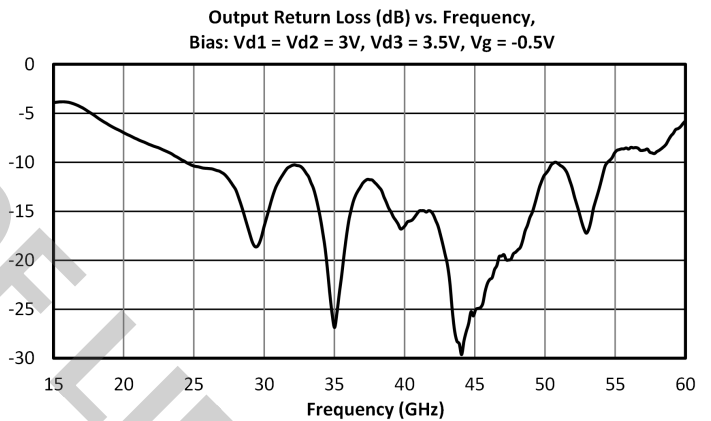
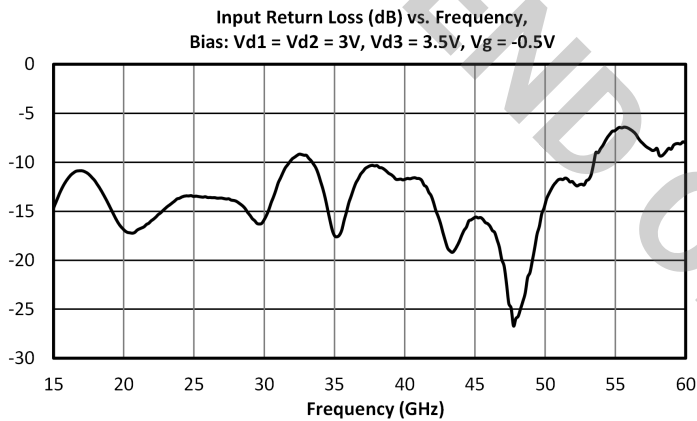
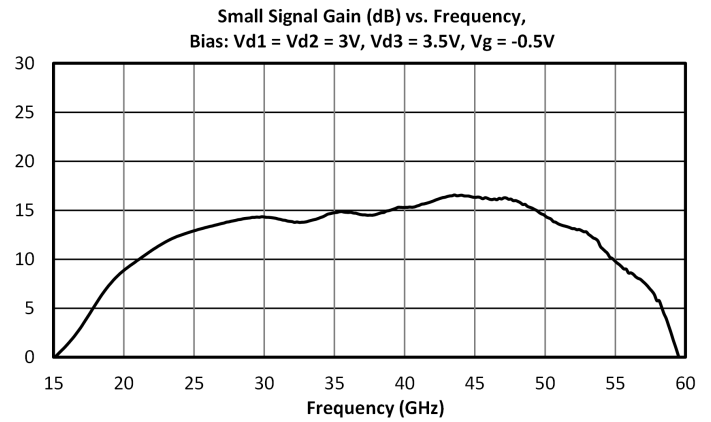
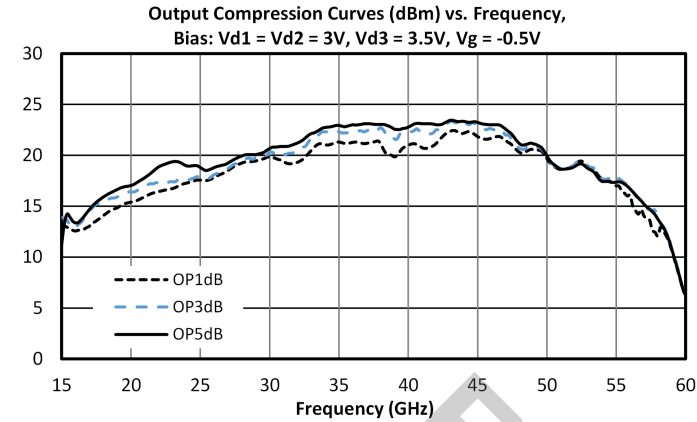
[1][2][3] Bias conditions for Id tested with no RF input power. See Typical Performance Plots for DC current vs. RF power. Bias conditions presented as Vd/Vg. Drain current is specified as Id1 + Id2 + Id3

[4][5][6] Saturated output power specification defined using the EVAL-APM-7210SM P5dB compression curve shown in Typical Performance Plots.

Typical Performance Plots , Bias: $V_{d1} = V_{d2} = 3V$, $V_{d3} = 3.5V$, $V_g = -0.5V$

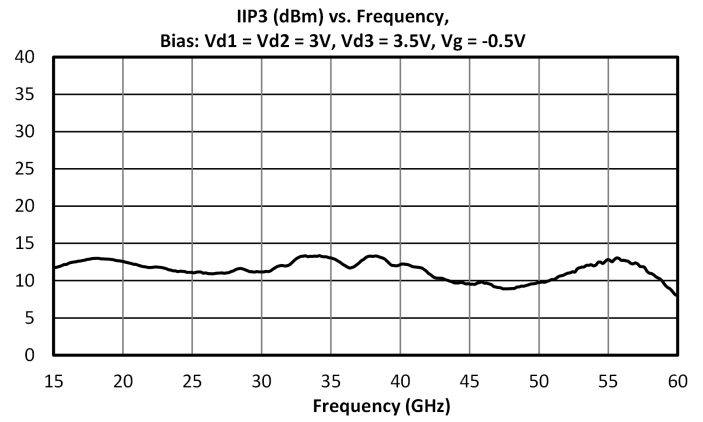
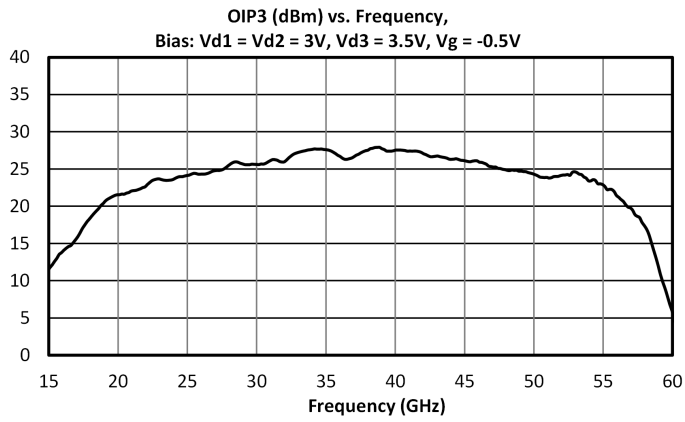
Measurement data taken using the EVAL-AMM-7210SM module.

Evaluation board losses are mathematically extracted out of Output Compression Curves, Small Signal Gain, Noise Figure, and IP3 plots.



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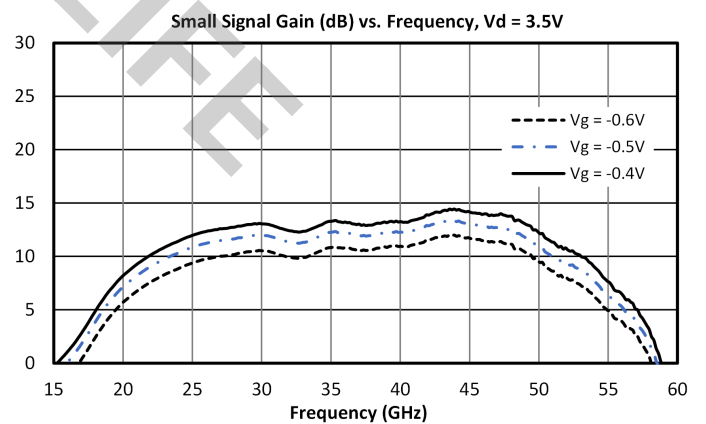
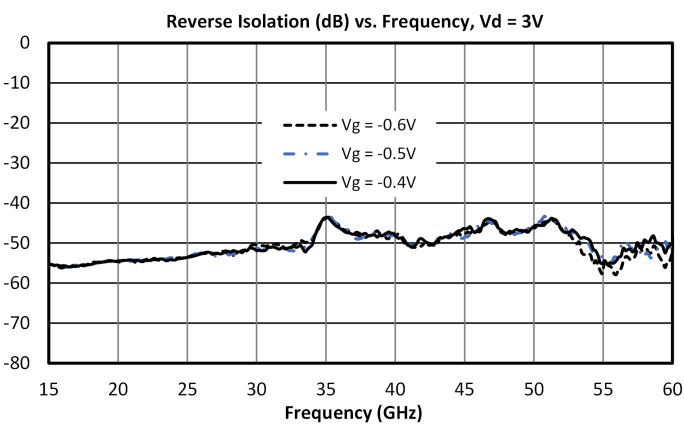
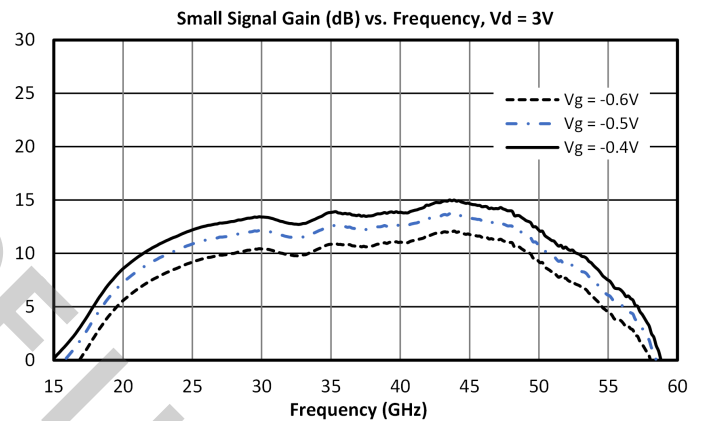
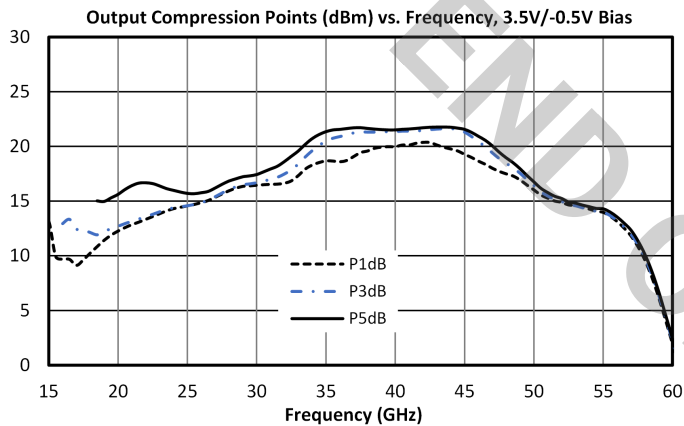
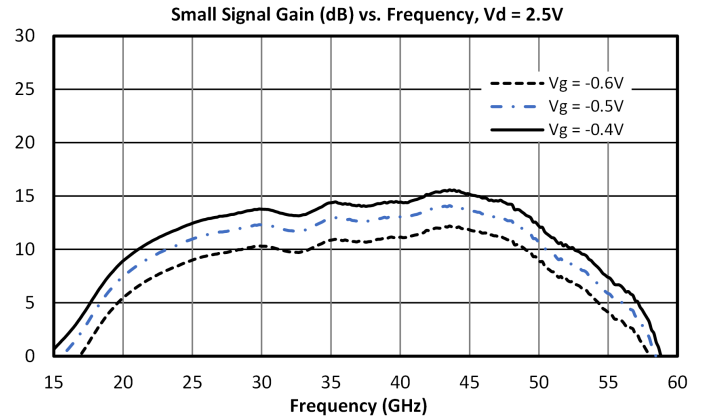
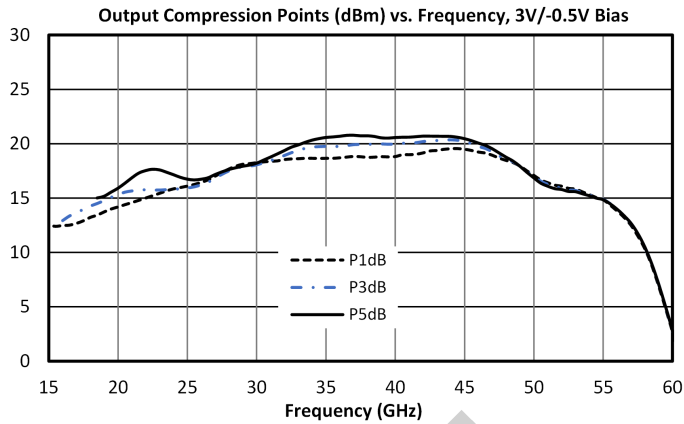


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Typical Performance Plots

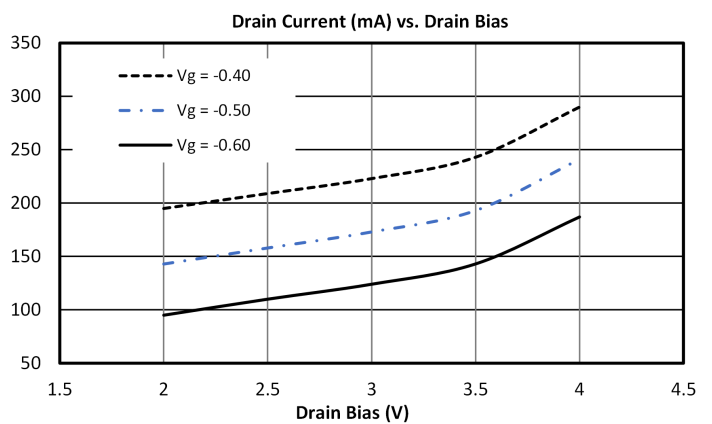
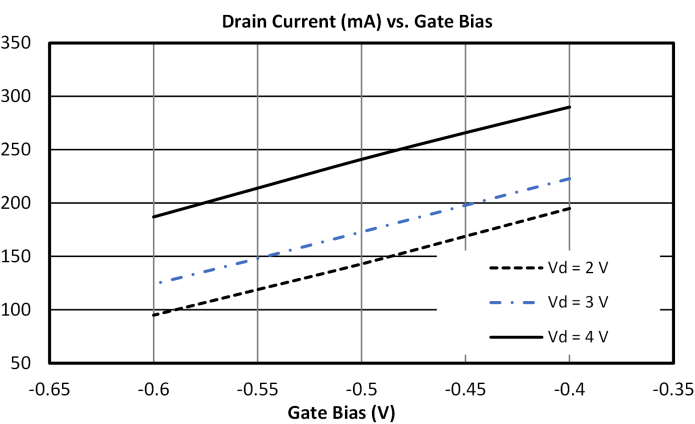
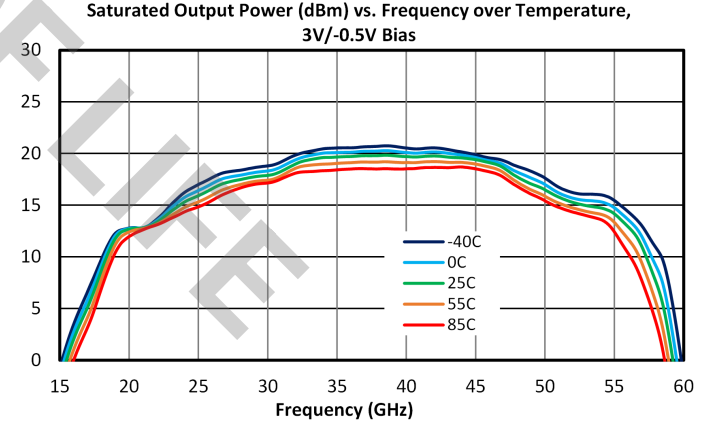
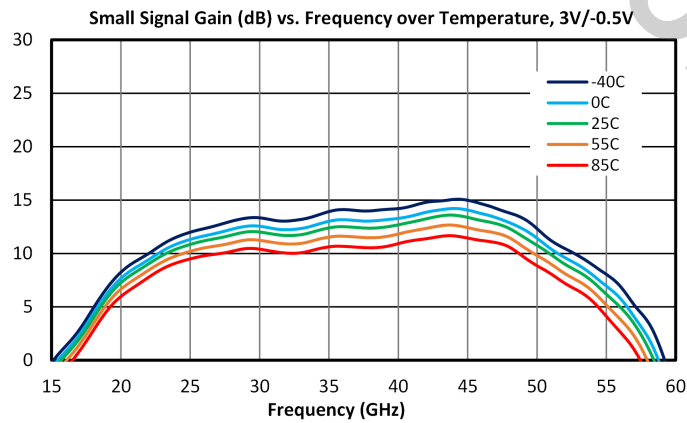
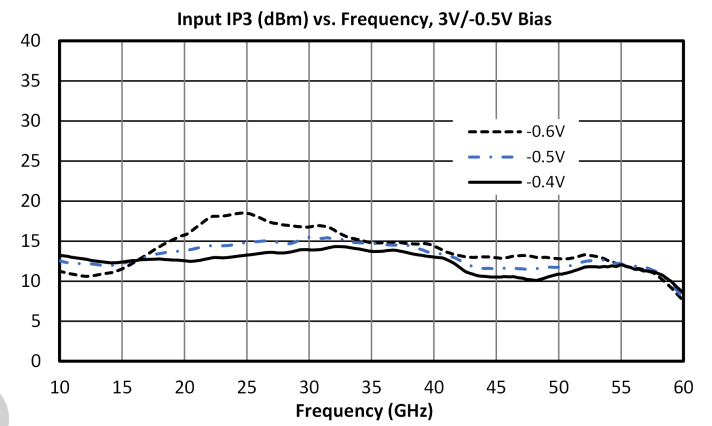
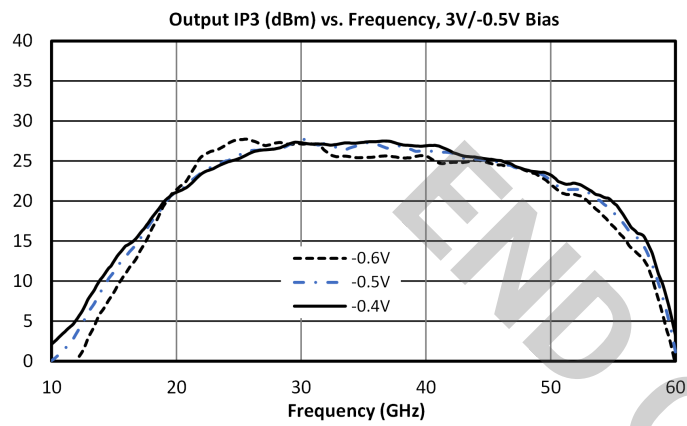
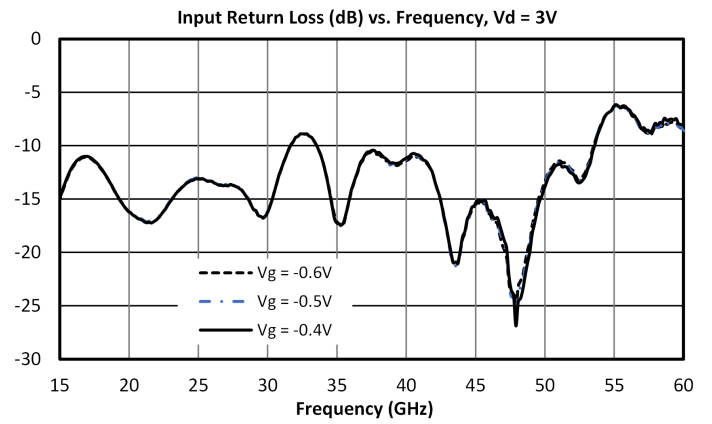
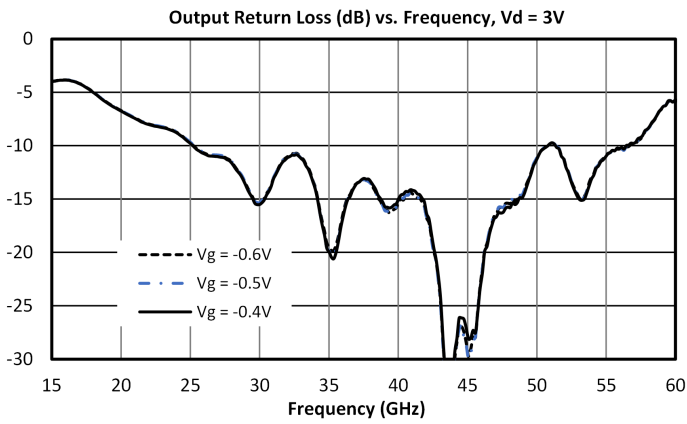
Measurement data taken using the EVAL-AMM-7210SM module.

¹⁴Drain current is specified as $I_{d1} + I_{d2} + I_{d3}$



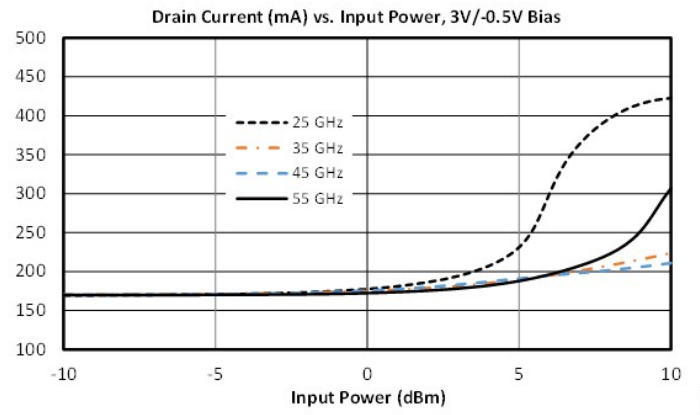
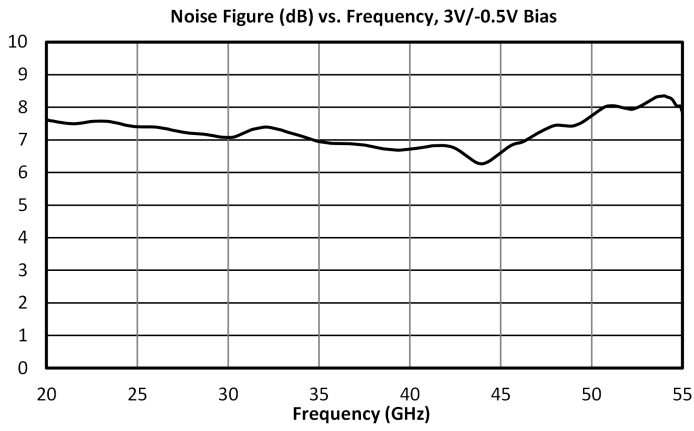
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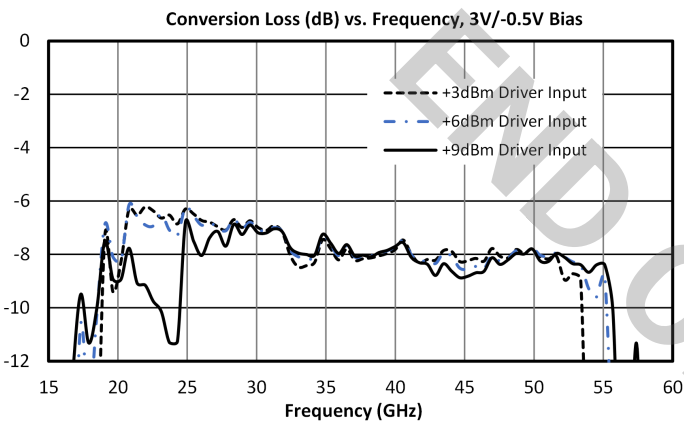
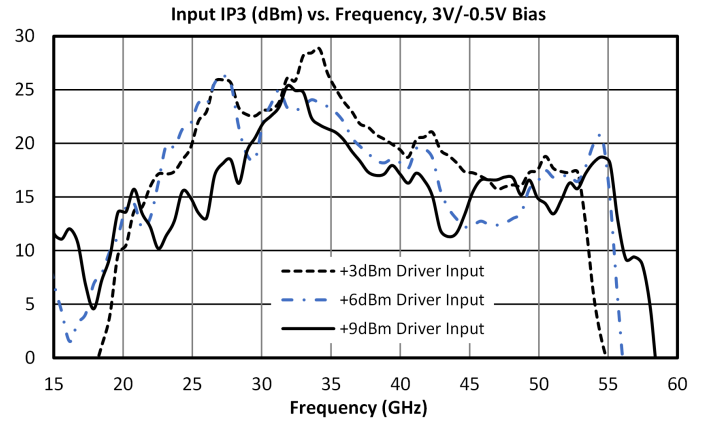
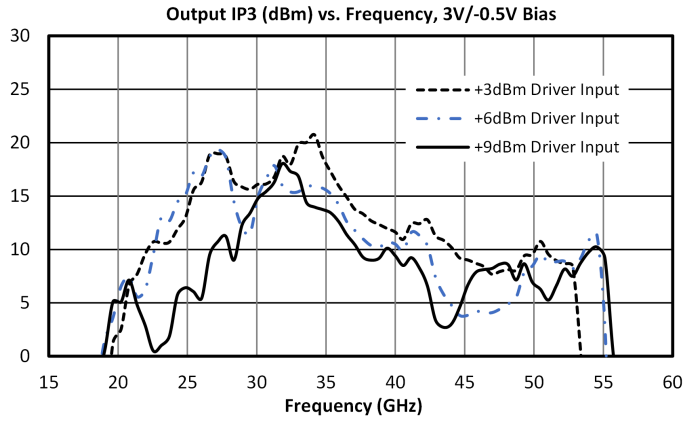
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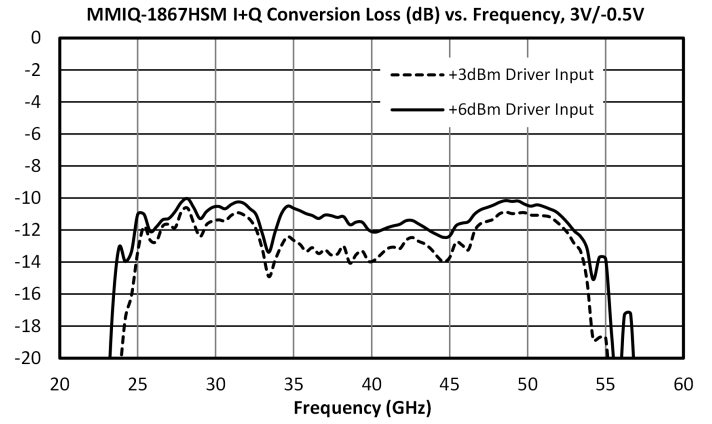
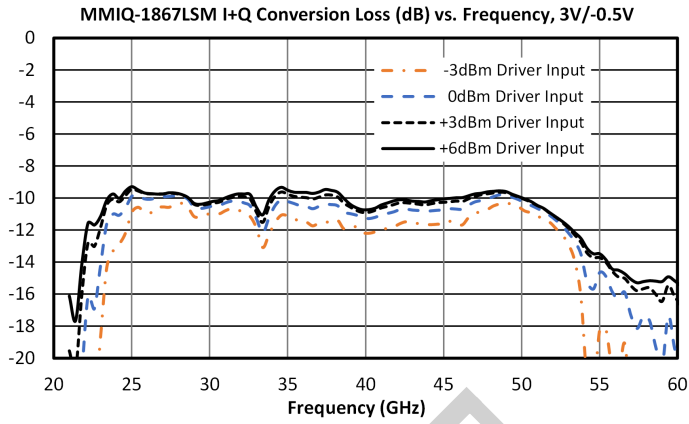
Typical Performance Plot of Marki MM1-1857H Using AMM-7210SM as LO Driver

Plots taken using EVAL-AMM-7210SM as LO driver for connectorized MM1-1857H module in configuration A with a 91MHz IF. Power specified is input power to EVAL-AMM-7210SM driver.



Typical Performance Plot of Marki MMIQ-1867LSM and MMIQ-1867HSM Using AMM-7210SM as LO Driver

Plots taken using EVAL-AMM-7210SM as LO driver for the EVAL-MMIQ-1867LSM in configuration A with a 6GHz IF. Power specified is input power to EVAL-AMM-7210SM driver.



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AMM-7210SM

25-50 GHz GaAs Surface Mount LO Driver
Amplifier

Application Information

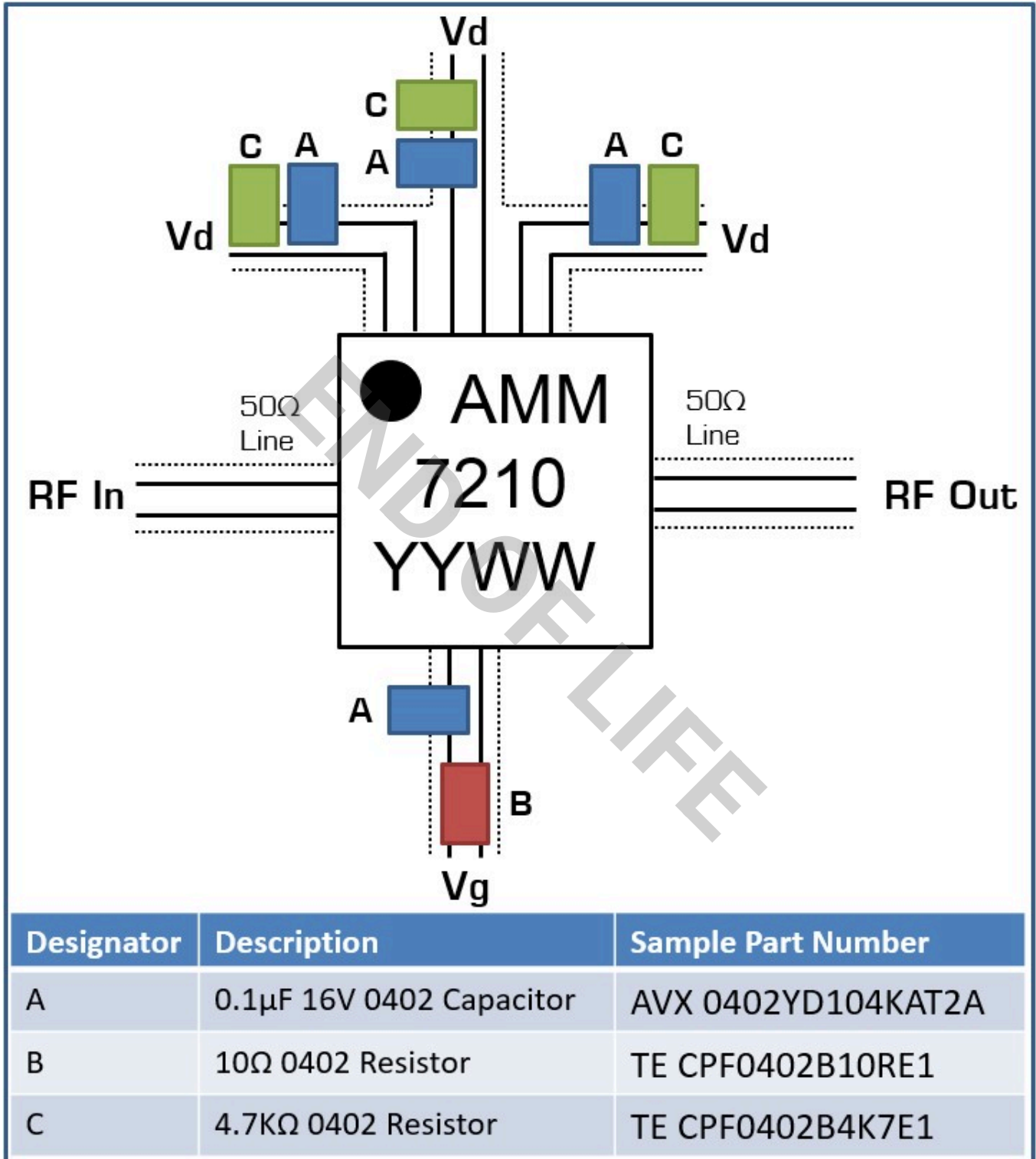
Below is the recommended application circuit for the AMM-7210SM:

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25-50 GHz GaAs Surface Mount LO Driver Amplifier

Application Circuit



AMM-7210SM

25-50 GHz GaAs Surface Mount LO Driver Amplifier

Application Circuit Description

The three Vd lines are separated to minimize feedback between the transistor's stages. The passive devices should be 0402 or 0201 surface mount. Examples of suitable passive devices would be the AVX 0402YD104KAT2A capacitor and TE CPF0402B10RE1 resistor. In addition to the resistor and capacitor on the gate pin, the layout of the board should be designed to minimize stray coupling between the drain and gate biasing traces on the board. Additionally, the gate biasing pin AMM-7210SM can draw up to 0.5mA at certain combinations of frequency and input power.

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Constant Current and Constant Voltage Operation

As with most amplifiers utilizing HEMT technology, the AMM-7210SM can be biased with a constant gate and drain voltage, or with a constant drain current by regulating the gate voltage. Using a constant gate and drain voltage for biasing reduces complexity, but has variable current consumption during operation. On the other hand, biasing the gate using a feedback network that samples the drain current minimizes unit-to-unit variation in gain and other parameters.

Under small signal excitation at a fixed temperature, these two approaches are equivalent. However, they will diverge in large signal conditions, where the drain current is affected by the frequency and power of the input signal. In these conditions P1dB, P3dB, and P5dB will be somewhat different, but based on tests with similar parts, they will be within a few dBm of the constant voltage curves.

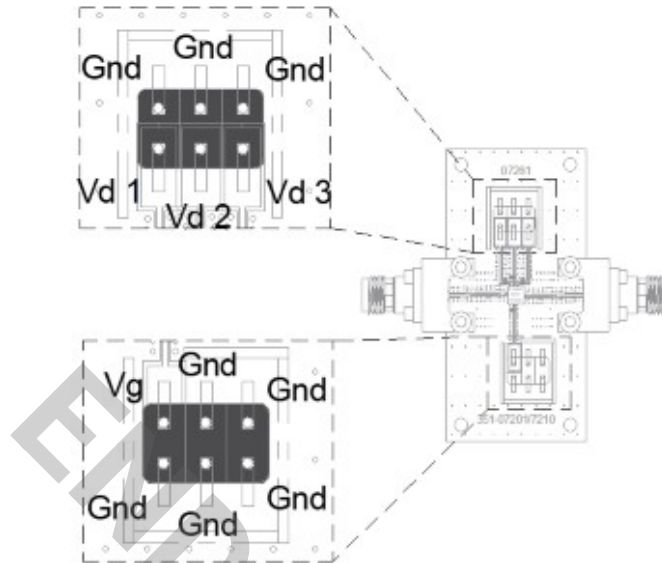
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Header Pinouts

On the EVAL-AMM-7210SM, there are two headers for biasing the drains and gates of the transistors. The pinout of the headers is given with their location on the evaluation board below:



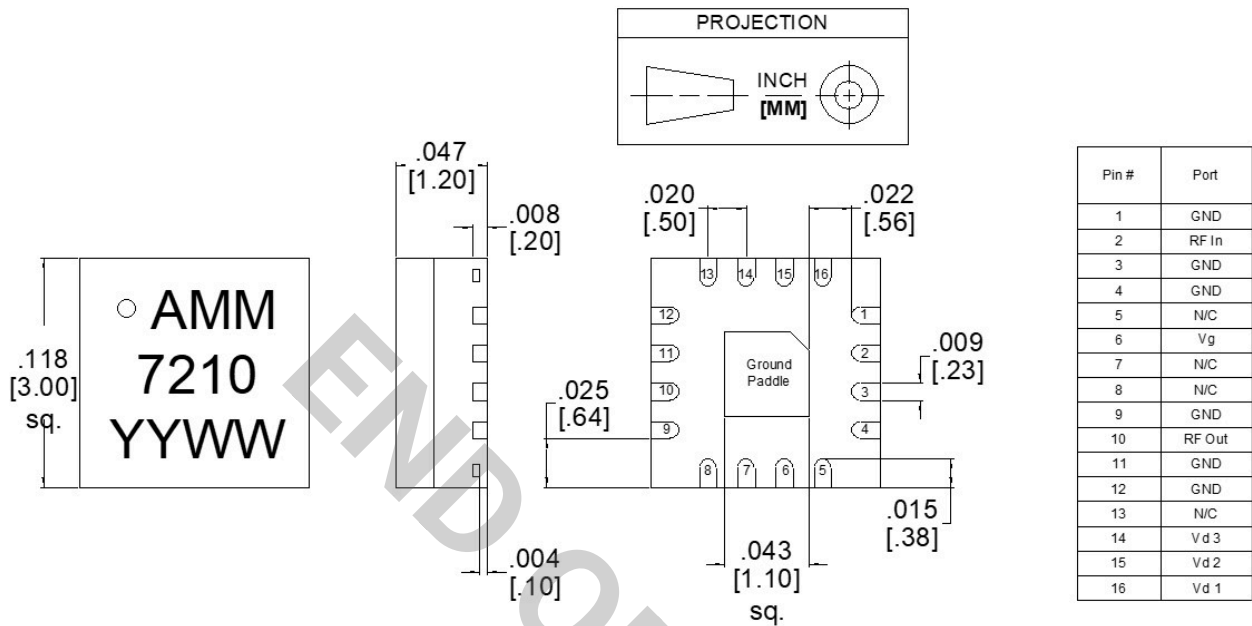
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Mechanical Data

Outline Drawing

Download : [Outline 3D Drawing](#) | [Outline 3D STP](#)



Notes:

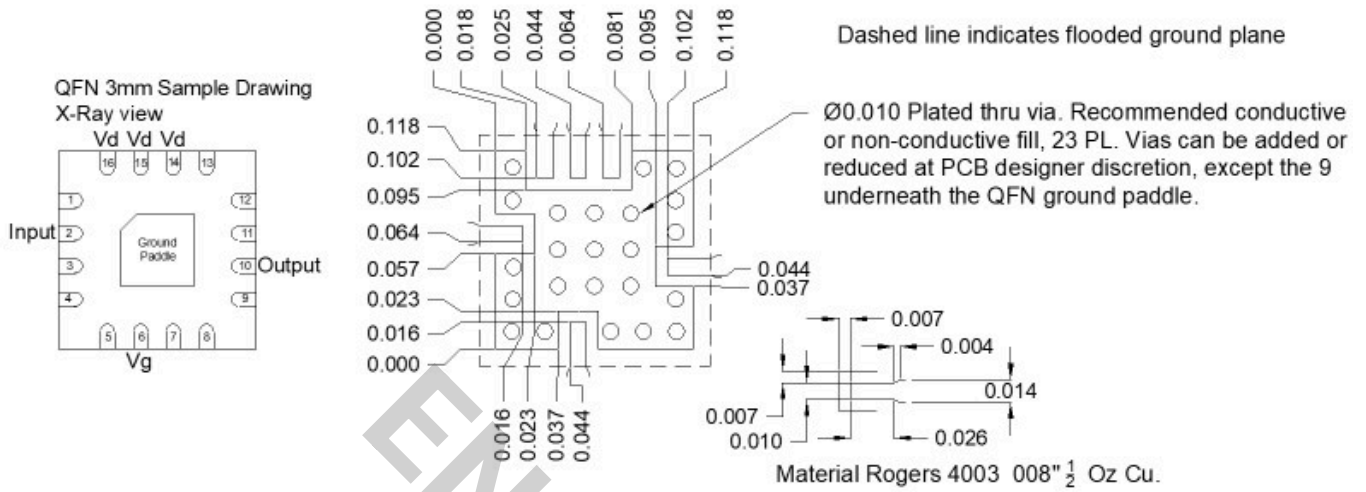
- 1) QFN material is plastic.
- 2) I/O Leads and Die Paddle are 0.05 microns Au over 0.02 microns Pd over 0.5 microns Ni
- 3) All unconnected pins should be connected to PCB RF ground.

AMM-7210SM

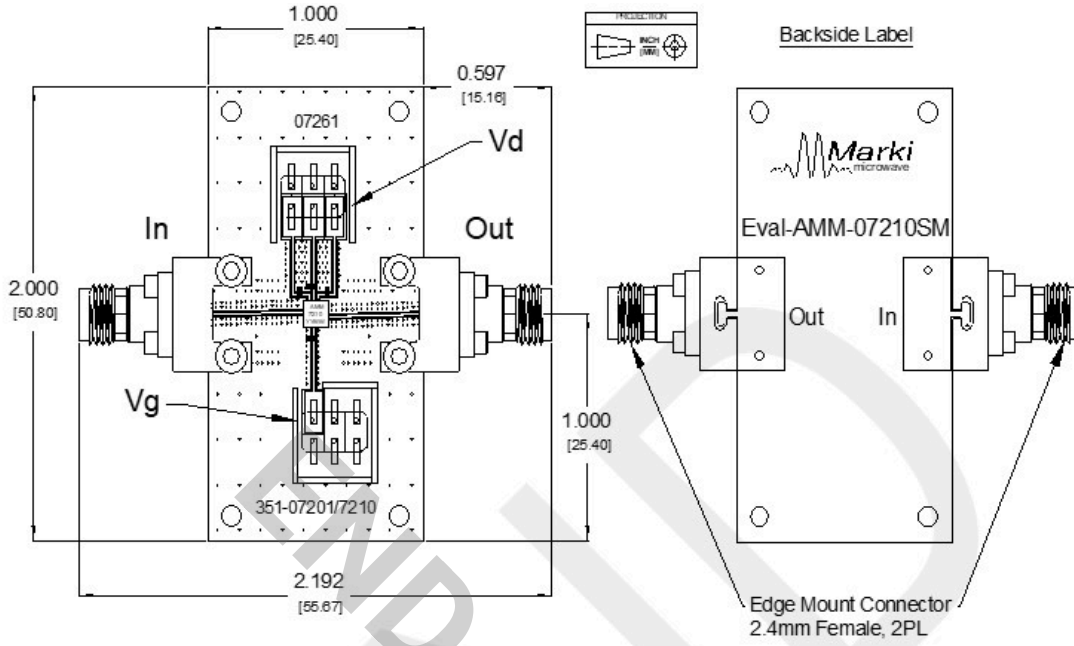
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Footprint Image

Download: [Footprint Drawing](#)



Evaluation Board - Outline Drawing



AMM-7210SM

25-50 GHz GaAs Surface Mount LO Driver Amplifier

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