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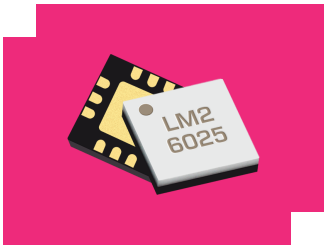
DLM-10SM

Tunable Differential Limiter

DEVICE OVERVIEW

General Description

The DLM-10SM is a tunable, dual channel GaAs Schottky diode signal limiter featuring excellent IP3, insertion loss, and return loss. The limiting level is adjustable with an off-chip bias network, and the two channels can be used for differential or single-ended signals. The DLM-10SM is available in a lead-free, RoHS compliant QFN surface mount package and is compatible with standard leaded and lead-free PCB reflow soldering processes. The DLM-10SM is a superior alternative to discrete diode limiting options.



Download s-parameters here

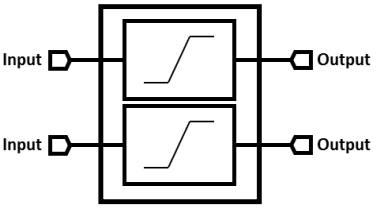
Features

- Industry leading IP3, low insertion loss and return loss
- Adjustable limiting level with off-chip bias network
- Single channel differential/Dual channel single ended
- RoHS Compliant

Applications

- RF Transceivers
- Test and Measurement Equipment
- SATCOM

Functional Block Diagram



Part Ordering Options

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
DLM-10SM	Tunable Differential Limiter	QFN	REACH RoHS	Released	EAR99
EVAL-DLM-10	Evaluation Board, Tunable Differential Limiter	EVAL	Consult Factory	Released	EAR99

Table Of Contents

Specifications

Absolute Maximum Ratings

Parameter	Maximum Rating	Unit
RF Power Handling , Average	0.5	W

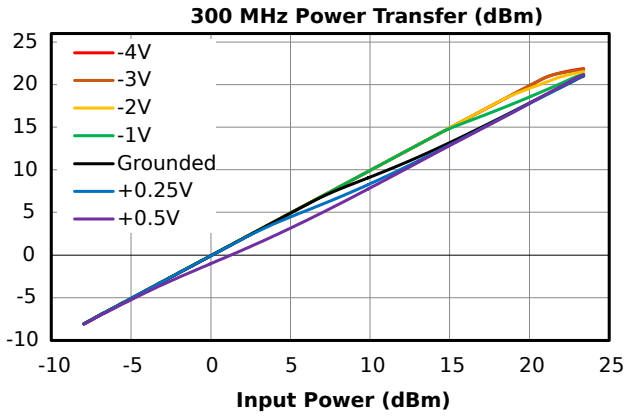
Package Information

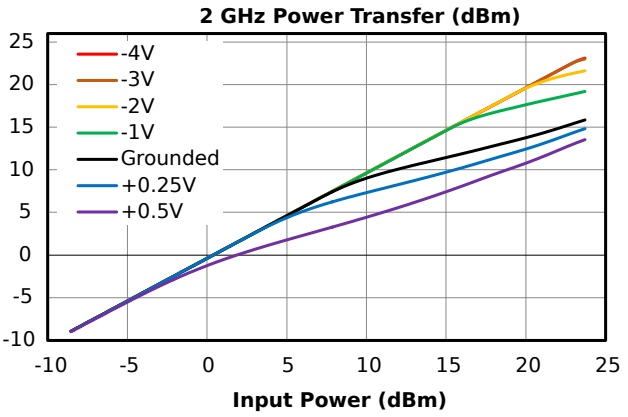
Parameter	Details	Rating
Dimensions	-	3 x 3 mm
Moisture Sensitivity Level	-	MSL 1

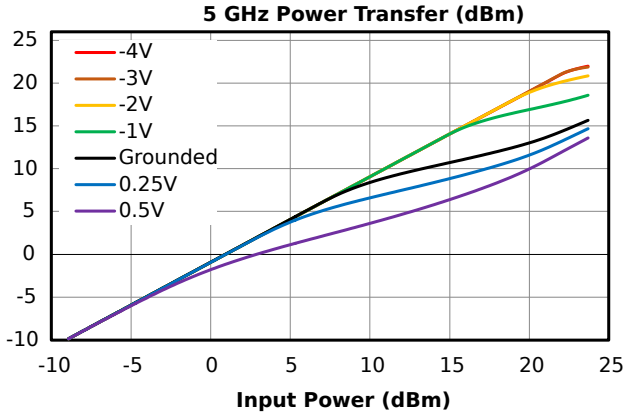
Electrical Specifications

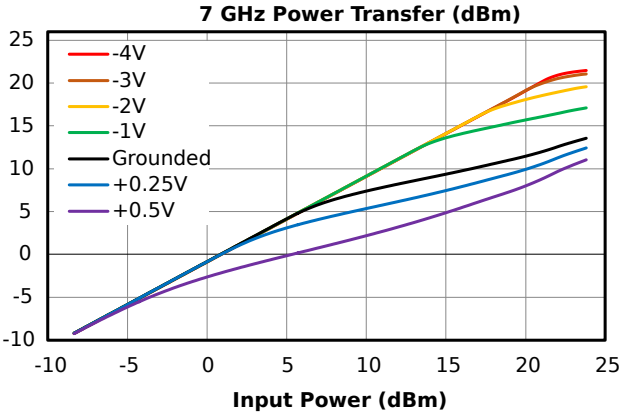
Parameter	Test Conditions	Minimum Frequency (GHz)	Maximum Frequency (GHz)	Min	Typ	Max	Unit
Input P1dB	Grounded Bias	0	10	-	10	-	dBm
Insertion Loss	+10dBm input power, grounded bias	0	10	-	1.4	-	dB
Insertion Loss	-10dBm input power, grounded bias	0	10	-	0.75	1.5	dB
Insertion Loss	+15dBm input power, grounded bias	0	10	-	3.75	-	dB
Return Loss	-10dBm to +9dBm, grounded bias	0	10	-	20	-	dB
Return Loss	+12dBm, grounded bias	0	10	-	15	-	dB

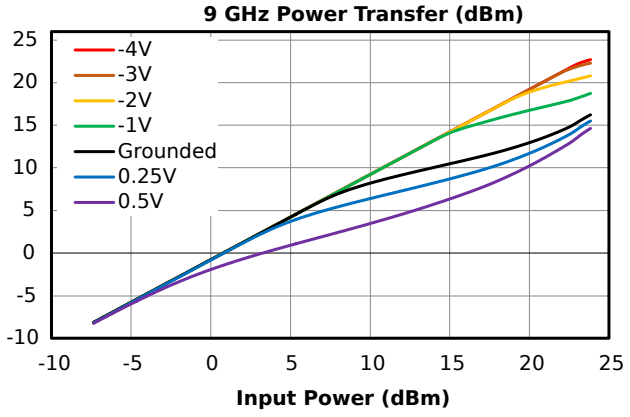
Typical Performance Plots

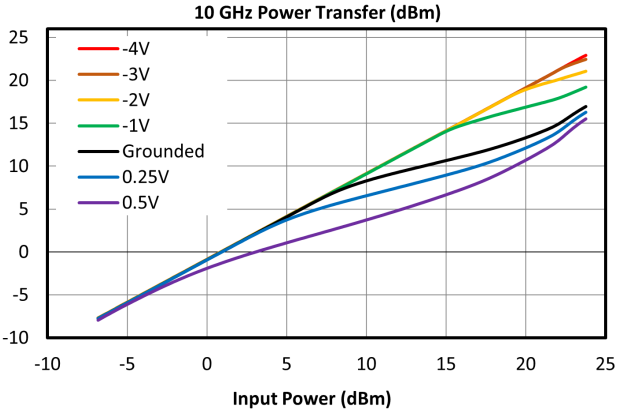


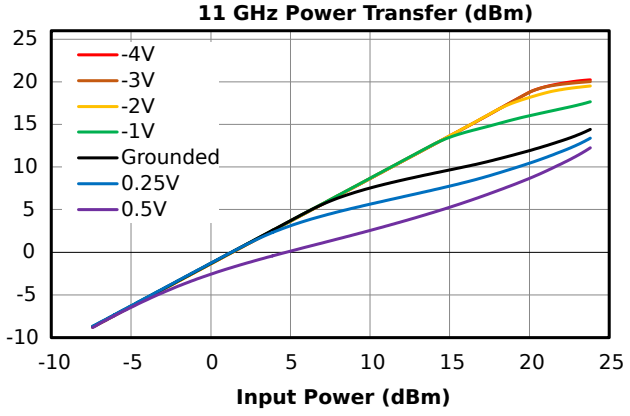


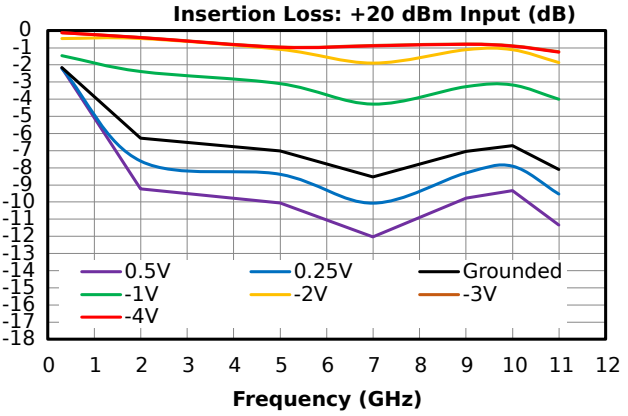


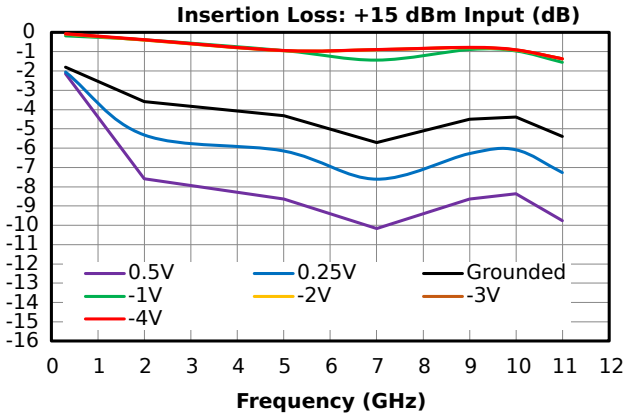


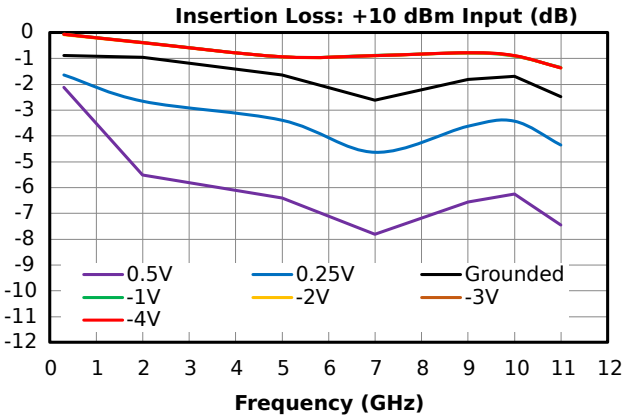


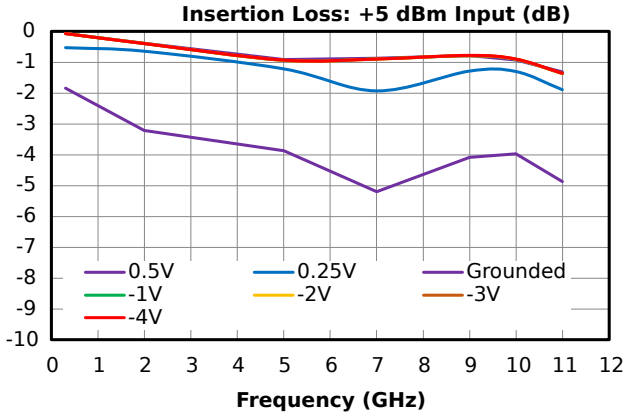


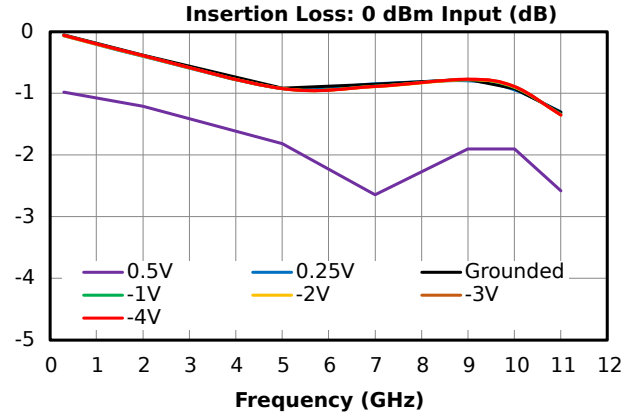


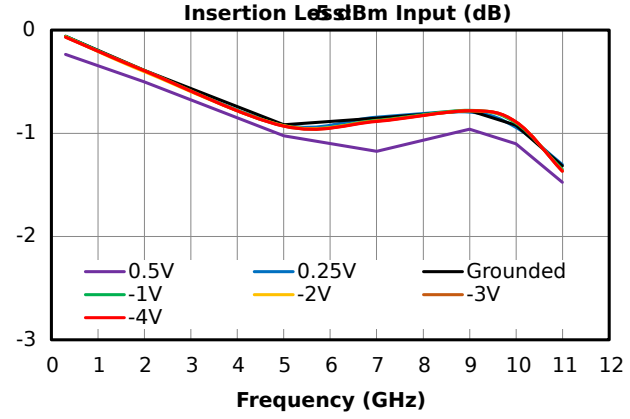


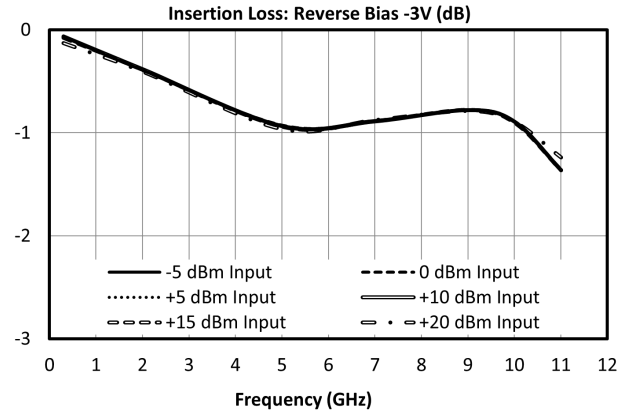


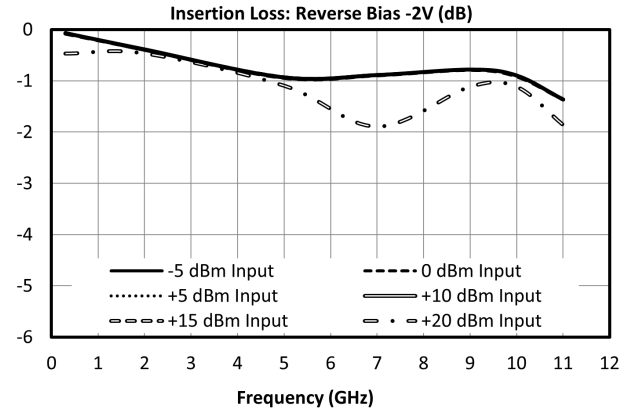


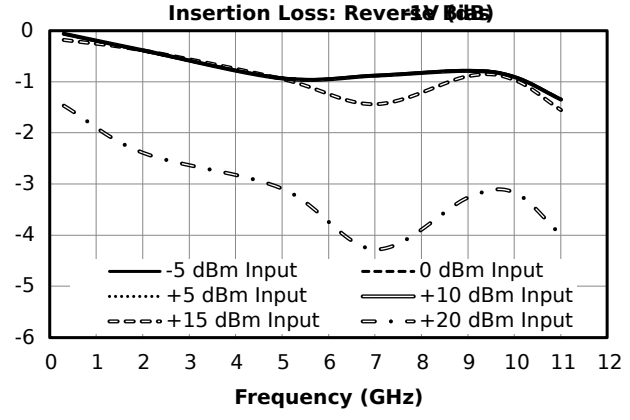


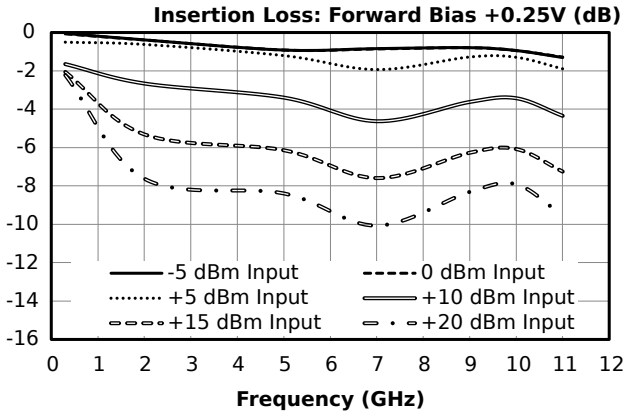


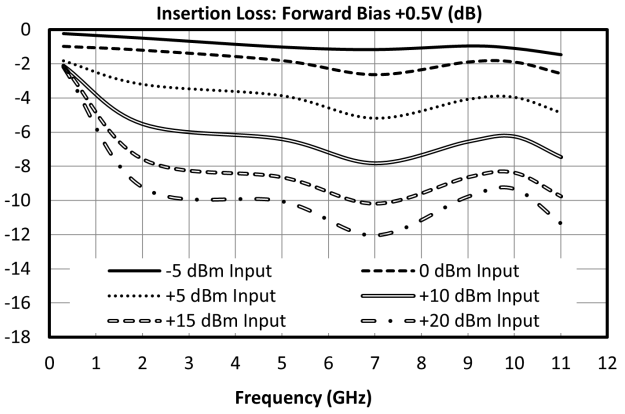


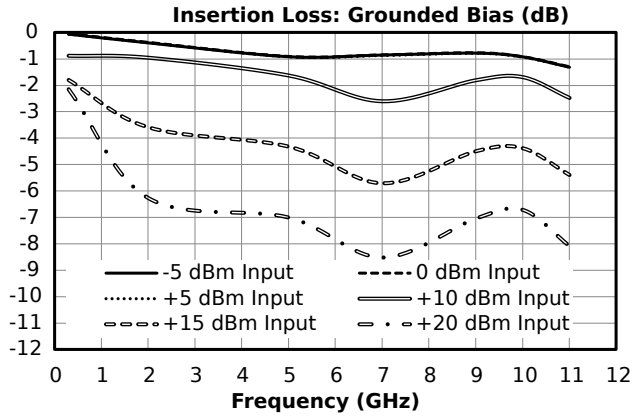


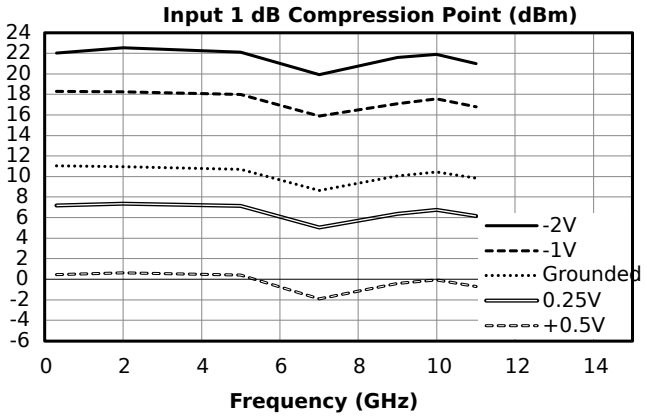






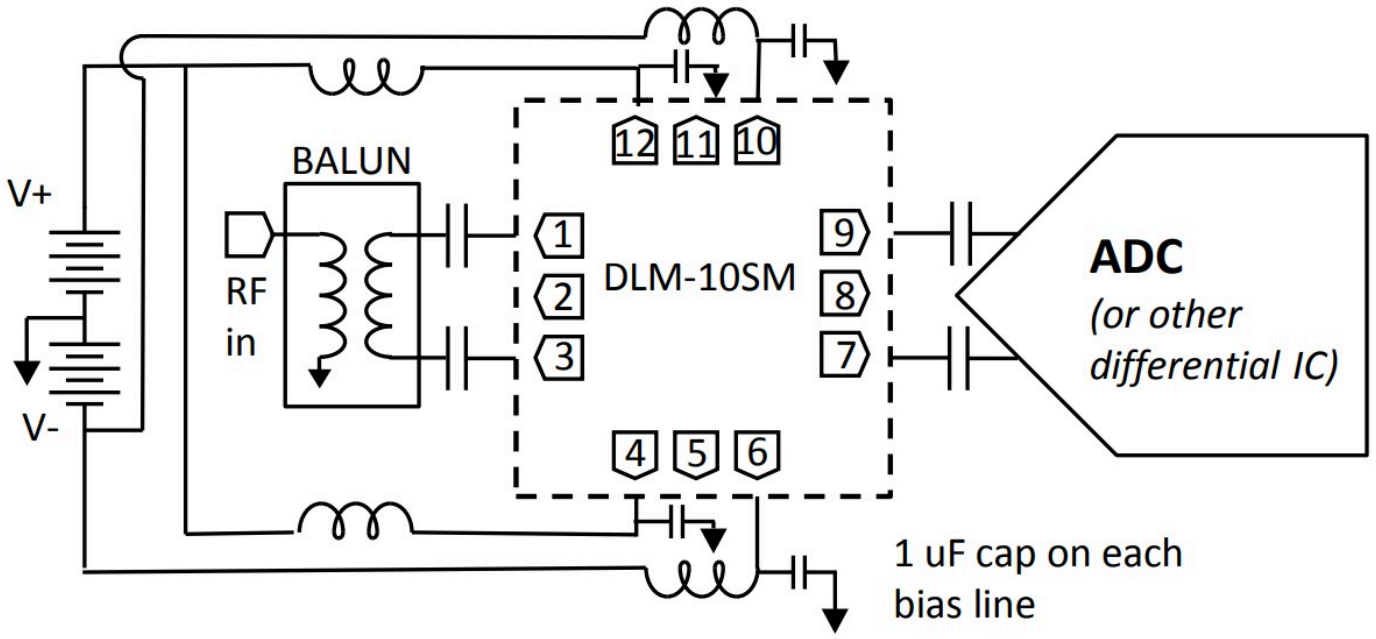






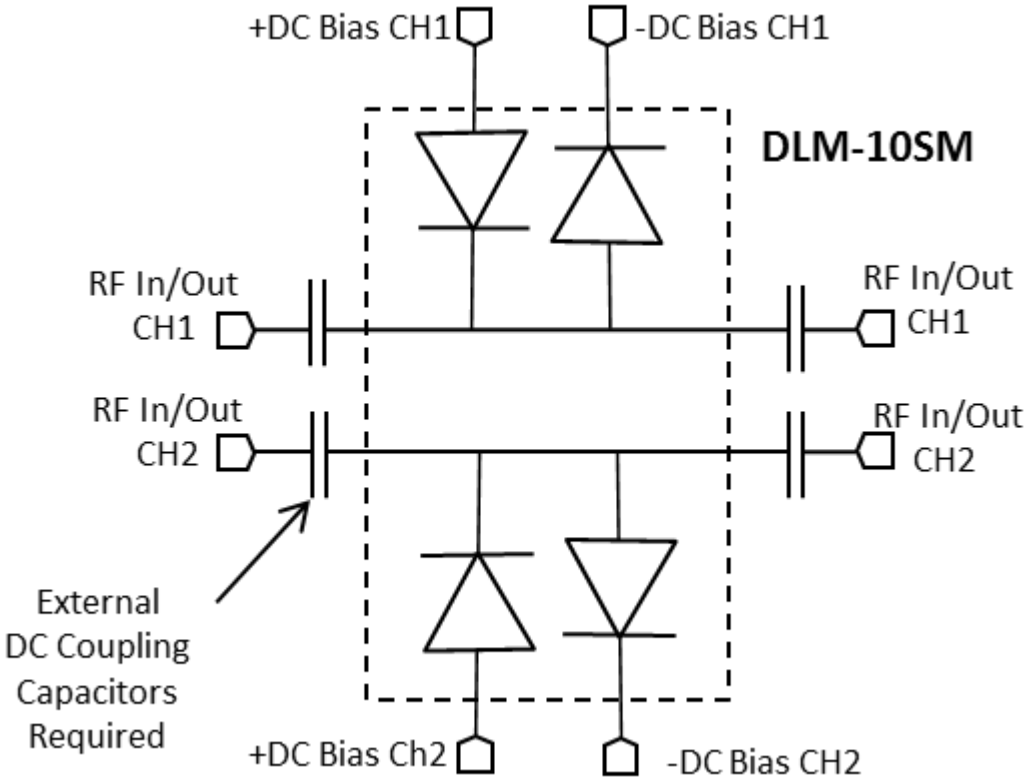
Application Information

Example Application Circuit



Differential/Two Channel Operation – The two limiting channels are not coupled together, so the device can be used as a singlechannel, two channel, or differential limiter. If the second channel is not used, it should be connected to RF ground.
Grounded Operation – Pins 4,6, 10, and 12 can be connected directly to RF/DC ground for ease of use. This will give a limitinglevel of around 7 dBm. If a higher or lower limiting level is desired, please see biased operation.
Biased Operation – For lower limiting levels, the internal diodes can be slightly forward biased to decrease the threshold voltage. Apositive voltage should be applied to Pins 12 and 4, and an equal negative voltage should be applied to pins 6 and 10 for symmetriclimiting. To increase the liminting threshold, the diodes should be reversed biased. This means that a negative voltage should be
applied to pins 12 and 4, and an equivalent positive voltage should be applied to pins 6 and 10.
Biasing Circuitry – A voltage/current source that can both source and sink current must be used. Many voltage leveling circuits can only supply current to set a minimum voltage. In this case the signal will cause the diodes to self-bias in limiting operation, increasing the bias threshold. The bias supply must be able to sink current to prevent self-biasing. A low impedance RF ground must be provided by bypass capacitors to ground as close as possible to the bias pins. High frequency bypass capacitors are included on chip, so only low frequency (~1uF) capacitors are necessary. The DC power supply should be decoupled from the limiter circuit through an RF choke and decoupling capacitors if necessary to eliminate power supply noise.

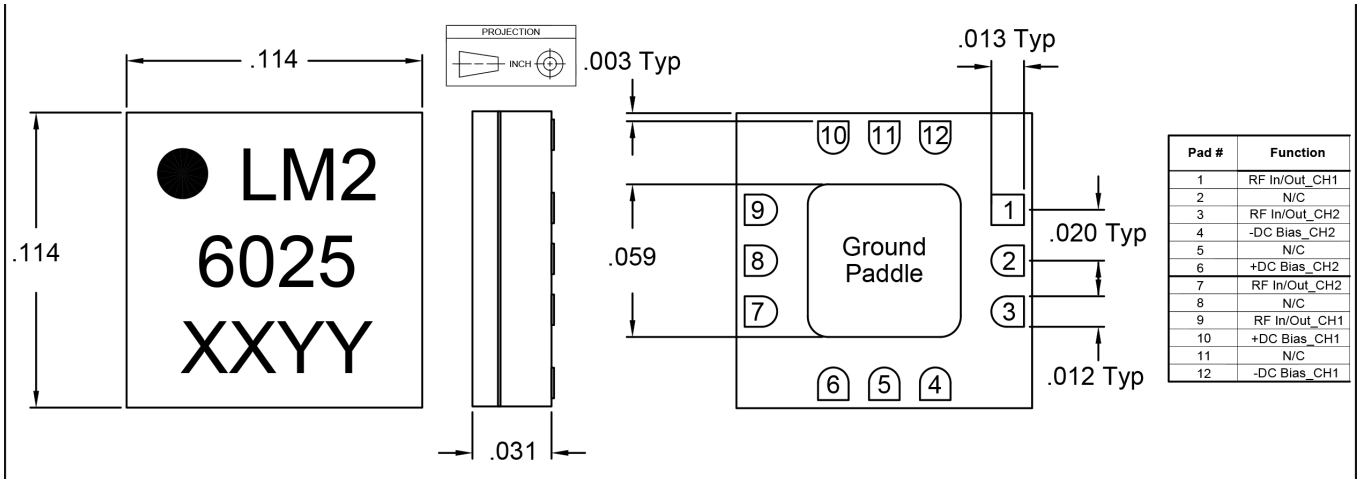
Application Circuit



Mechanical Data

Outline Drawing

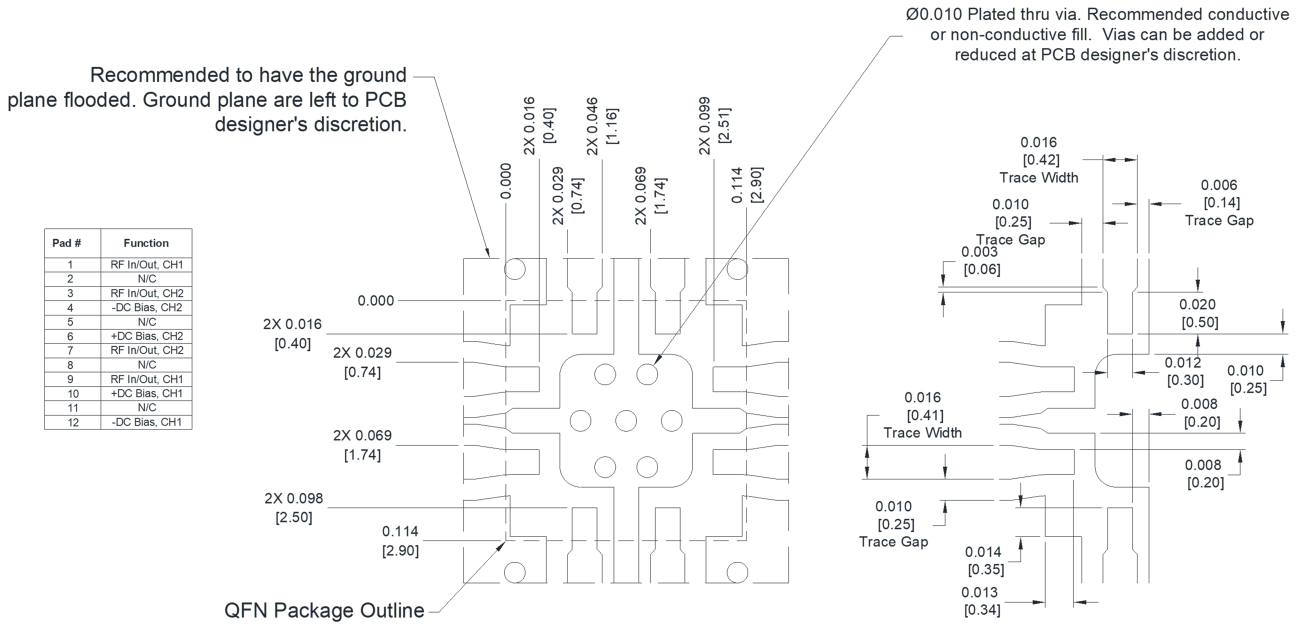
Download : Outline 2D Drawing | Outline 3D Drawing | Outline 3D STP



Pad #	Function
1	RF In/Out_CH1
2	N/C
3	RF In/Out_CH2
4	-DC Bias_CH2
5	N/C
6	+DC Bias_CH2
7	RF In/Out_CH2
8	N/C
9	RF In/Out_CH1
10	+DC Bias_CH1
11	N/C
12	-DC Bias_CH1

Footprint Image

Download : Footprint Drawing



Pad #	Function
1	RF In/Out, CH1
2	N/C
3	RF In/Out, CH2
4	-DC Bias, CH2
5	N/C
6	+DC Bias, CH2
7	RF In/Out, CH2
8	N/C
9	RF In/Out, CH1
10	+DC Bias, CH1
11	N/C
12	-DC Bias, CH1

The Landing Pattern is to be used on Rogers 4003, 0.008" thick $\frac{1}{2}$ Oz Copper both sides.

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