

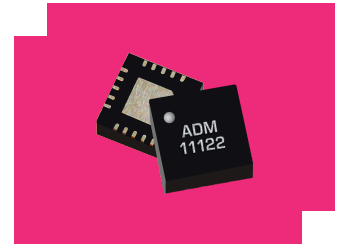
ADM-11122PSM

2 - 20 GHz, Wideband High OIP2 Amplifier

DEVICE OVERVIEW

General Description

The ADM-11122PSM is a surface-mount, wideband, high output IP2, gain block amplifier designed to operate from 2 to 20 GHz. It provides 19 dB typical small-signal gain across the band, along with 4.2 dB typical noise figure and 13.7 dBm typical output P1dB. The amplifier also delivers 55 dBm typical output IP2, making it well suited for direct-conversion EW systems and other wideband signal chain applications where gain and second-order linearity are critical. The device is internally matched to 50 ohms at both input and output, and operates with a +4 V supply voltage, drawing just 84 mA. The ADM-11122PSM is packaged in a compact 4 x 4 mm plastic QFN for easy integration with automated assembly processes.



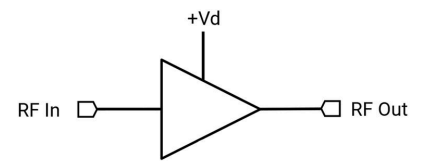
Features

- Ultra High Output IP2, +55 dBm Typical
- High Gain, 19 dB Typical
- Minimal Application Circuit
- Single Positive Supply Voltage, +4 V

Applications

- Electronic Warfare
- Direct Conversion Systems

Functional Block Diagram



Part Ordering Options

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
ADM-11122PSM	2 - 20 GHz, Wideband High OIP2 Amplifier	Plastic QFN	REACH RoHS	Released	EAR99
EVB-ADM-11122P	Evaluation Board, 2-20 GHz Wideband High OIP2 Amplifier	EVB	REACH RoHS	Released	EAR99

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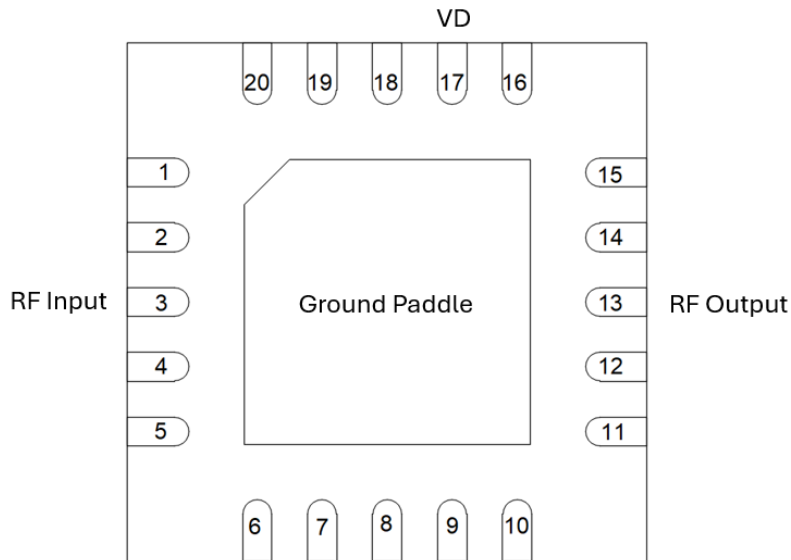
Revision History

Revision Code	Revision Date	Comment
-	2026-03-27	Initial Release

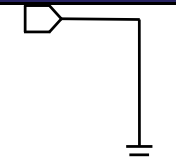
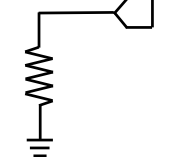
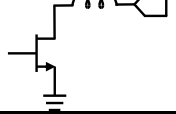
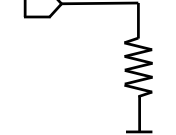
Port Configuration and Functions

Port Diagram

Below is the port configuration diagram for the ADM-11122PSM (X-ray view).



Port Functions

Port	Function	Description	DC Equivalent Circuit
Ground Paddle	Ground	Ground paddle and non-connected pins must be connected to a DC/RF ground potential with high thermal and electrical conductivity, and low inductance.	
Pin 13	RF Output	Pin 13 is the amplifier's RF output pin. This port is internally matched to 50 Ohms and is internally DC shorted to GND. This pin may be left floating if no DC is present on the line but should be DC blocked otherwise.	
Pin 17	Vd	Pin 17 is the DC bias supply for the amplifier. The voltage at this pin should be set to 4V for normal operation. This part requires an off-chip bypass capacitor of 0.1uF installed at this pin as close to the IC as possible. See applications circuit.	
Pin 3	RF Input	Pin 3 is the amplifier's RF input pin. This port is internally matched to 50 Ohms and is internally DC shorted to GND. This pin may be left floating if no DC is present on the line but should be DC blocked otherwise.	

Specifications

Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If these limits are exceeded, the device may be inoperable or have a reduced lifetime. This amplifier is designed and characterized in a 50Ω system, and operation in a reflective environment can cause performance degradation.

Parameter	Maximum Rating	Unit
Maximum Operating Temperature	85	°C
Maximum Storage Temperature	150	°C
Max Junction Temperature for MTTF > 1E6 hours	175	°C
Minimum Operating Temperature	-40	°C
Minimum Storage Temperature	-65	°C
Positive Drain Supply Current (with RF Input)	134	mA
Positive Drain Supply Voltage (Vd)	6	V
RF Input Power	10	dBm
Thermal Resistance, θ_{JC}	50	°C/W

Package Information

Parameter	Details	Rating
ESD	250 to < 500 Volts	HBM Class 1A
Dimensions	-	4 x 4 mm
Moisture Sensitivity Level	-	MSL 1

Recommended Operating Conditions

The Recommended Operating Conditions indicate the limits, inside which the device should be operated, to guarantee the performance given in Electrical Specifications. Operating outside these limits may not necessarily cause damage to the device, but the performance may degrade outside the limits of the Electrical Specifications. For limits, above which damage may occur, see Absolute Maximum Ratings .

Parameter	Min	Nominal	Max	Unit
Positive DC Current (Id) (No RF Input)	60	84	107	mA
Ambient Temperature	-40	25	85	°C
Power Supply DC Voltage	3	4	5	V

Sequencing Requirements

There are no sequencing requirements to power up or power down the amplifier.

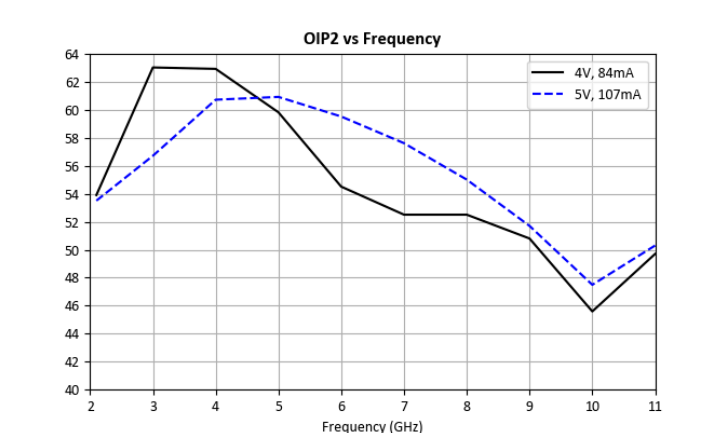
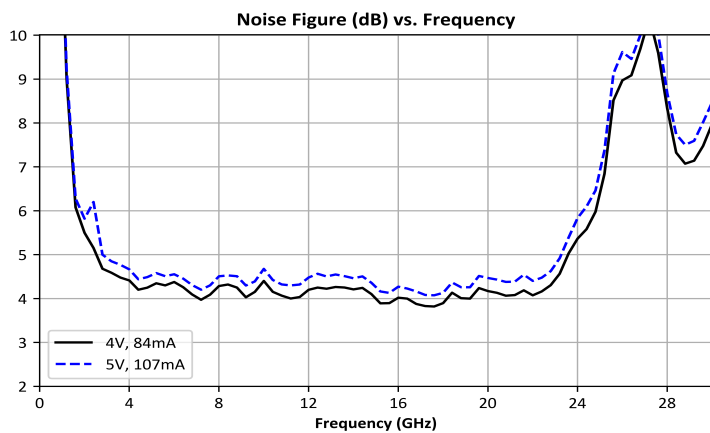
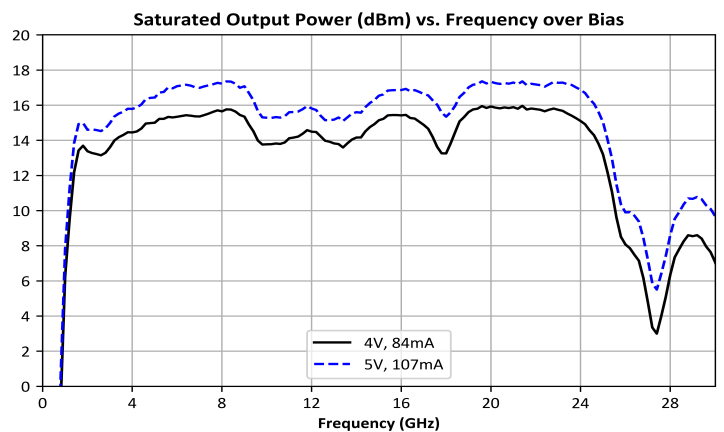
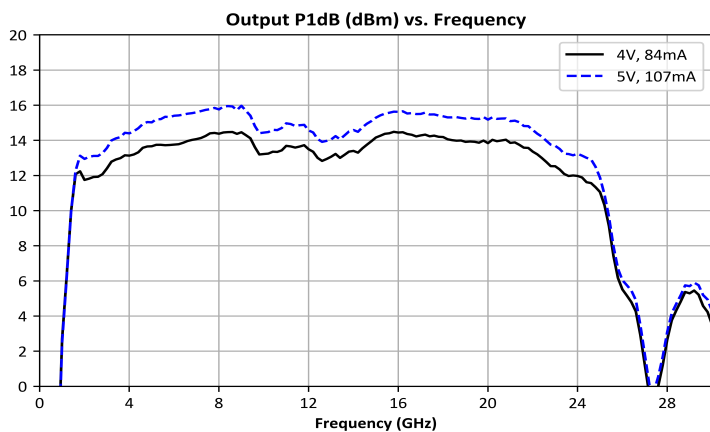
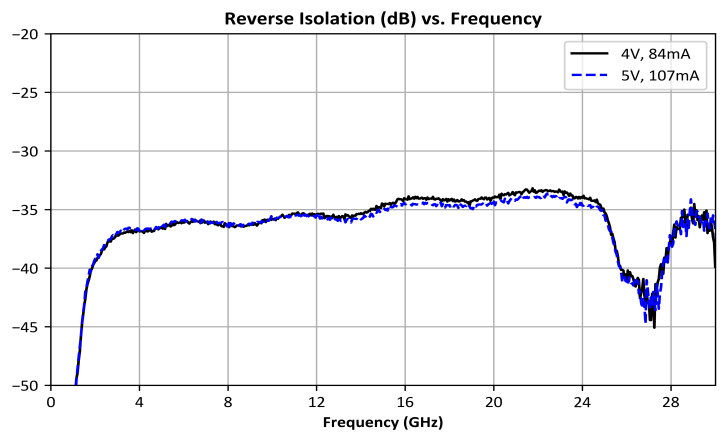
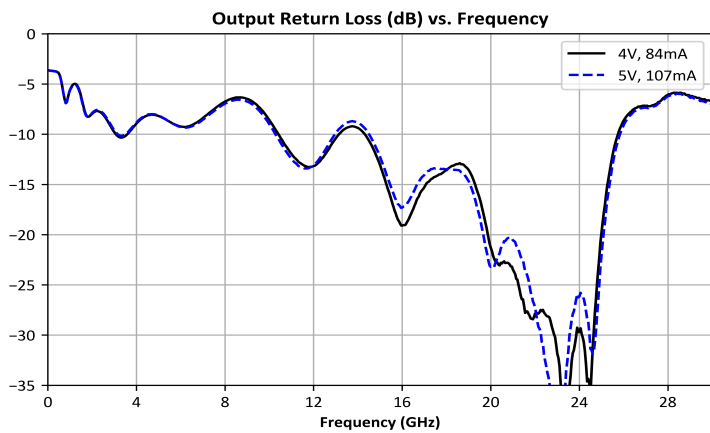
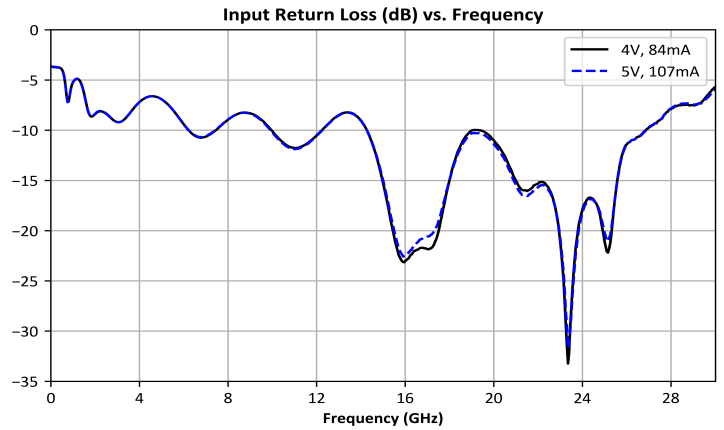
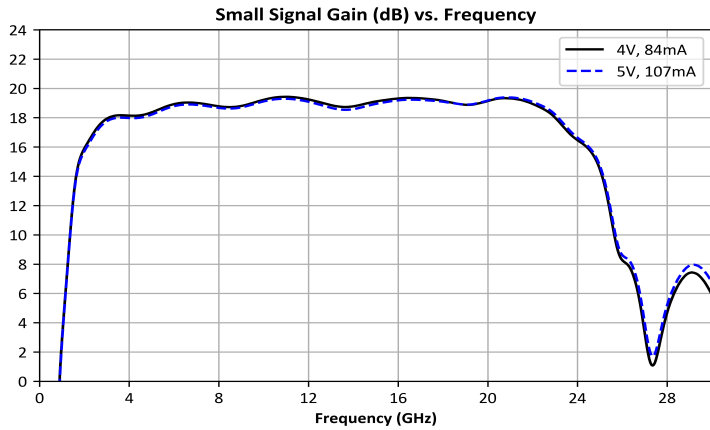
Electrical Specifications

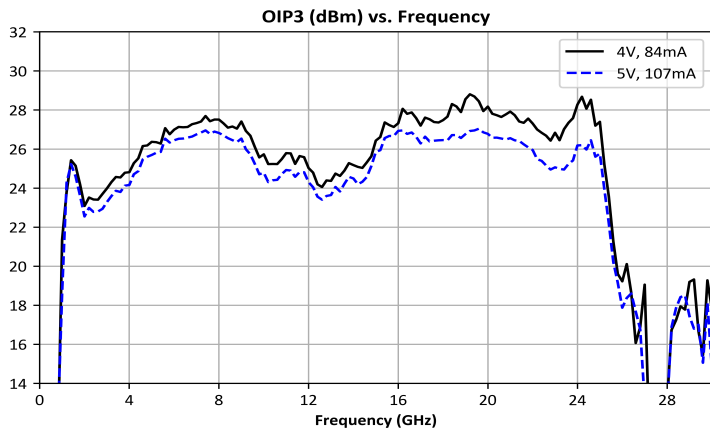
The electrical specifications apply at TA=+25°C in a 50Ω system. QFNs are 100% RF tested.

Parameter	Test Conditions	Minimum Frequency (GHz)	Maximum Frequency (GHz)	Min	Typ	Max	Unit
Small Signal Gain	Vd = 4V, Id = 84mA, -25dBm input power	2	20	-	19	-	dB
Input Return Loss	Vd = 4V, Id = 84mA, -25dBm input power	2	20	-	10	-	dB
Output Return Loss	Vd = 4V, Id = 84mA, -25dBm input power	2	20	-	10	-	dB
Reverse Isolation	Vd = 4V, Id = 84mA, -25dBm input power	2	20	-	35	-	dB
Noise Figure	Vd = 4V, Id = 84mA	2	20	-	4.2	-	dB
Output P1dB	Vd = 4V, Id = 84mA	2	20	-	13.7	-	dBm
Saturated Output Power	Vd = 4V, Id = 84mA	2	20	-	14.7	-	dBm
Output IP2	Vd = 4V, Id = 84mA, -25dBm input tone power, 1 MHz spacing	2	11	-	55	-	dBm
Output IP3	Vd = 4V, Id = 84mA, -15dBm input tone power, 1 MHz spacing	2	20	-	26	-	dBm
Input IP3	Vd = 4V, Id = 84mA, -15dBm input tone power, 1 MHz spacing	2	20	-	7.6	-	dBm
Current Consumption ¹	VD = 4V	-	-	-	84	-	mA

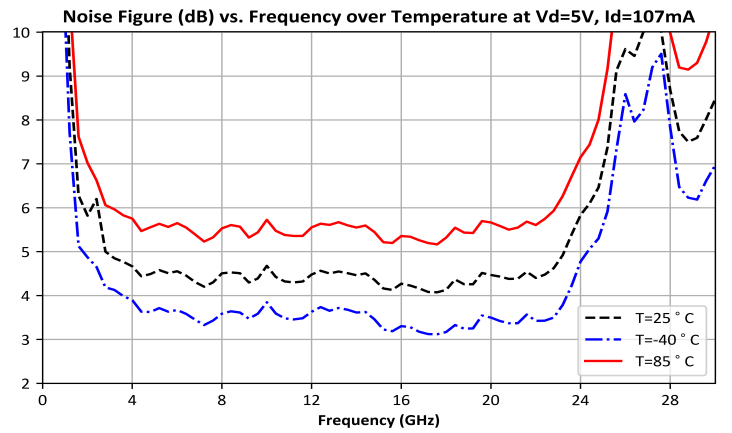
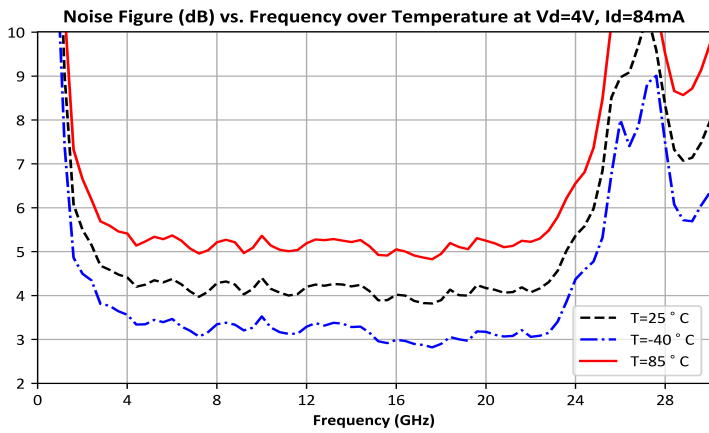
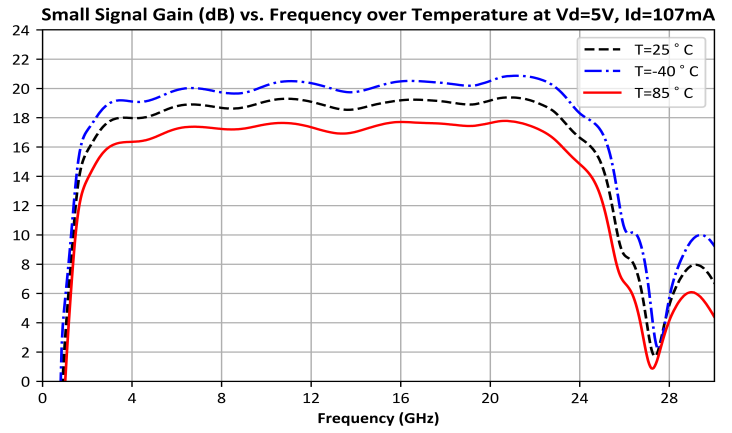
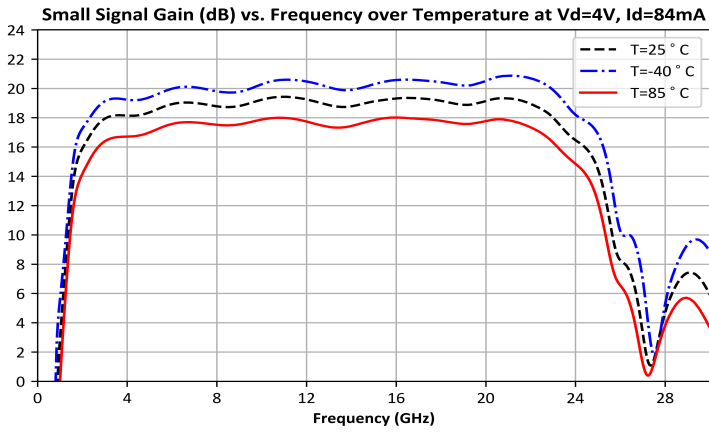
^[1] Bias conditions for Id tested with no RF input power.

Typical Performance Plots (vs Bias)





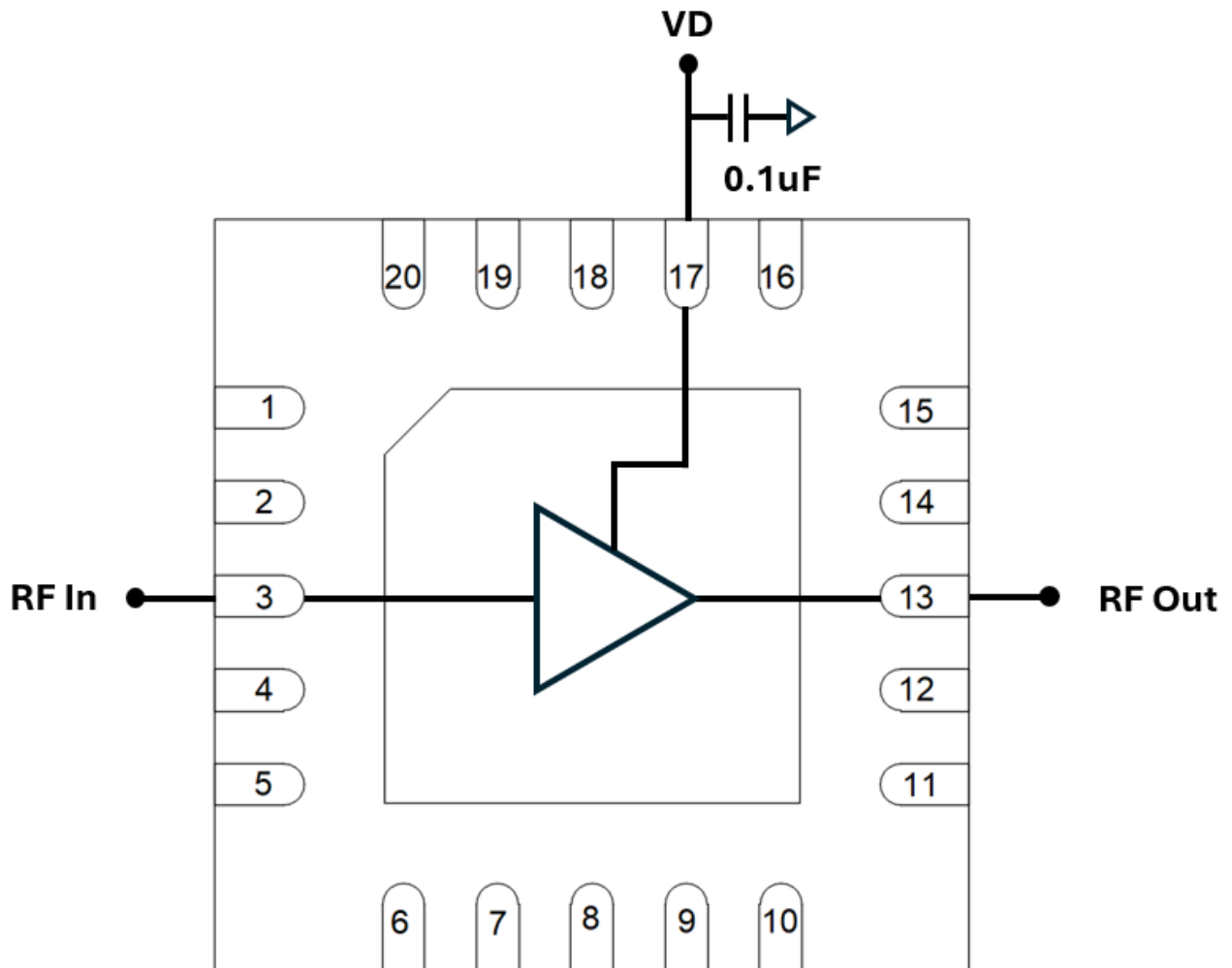
Typical Performance Plots (vs Temperature)



Application Information

Below is the recommended application circuit for the ADM-11122PSM. This is the configuration that is used to characterize this device. However, each PCB layout and environment are different which may require minor modifications of the biasing network. Please contact support@markimicrowave.com for more information.

Application Circuit




Application Circuit Description

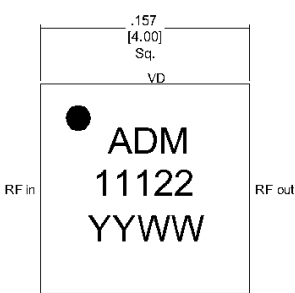
Above is the recommended application circuit for the ADM-11122PSM. DC drain voltage is supplied to the amplifier across a 0.1uF bypass capacitor to the Vd pin. The RF input and output ports are internally DC shorted to GND. These pins may be left floating if no DC is present on the line but should be DC blocked otherwise.

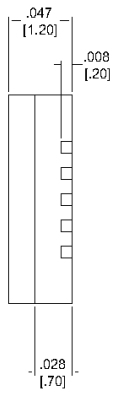
Mechanical Data

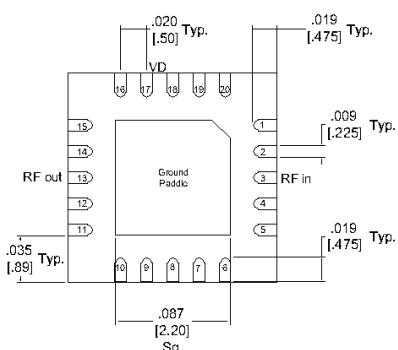
Outline Drawing

Download : [Outline 2D Drawing](#) | [Outline 3D Drawing](#) | [Outline 3D STP](#)

PROJECTION		REVISIONS			
	INCH [MM]	REV.	DESCRIPTION	DATE	APPROVALS
		A	Initial Release	3/16/26	AT








Pin #	Function
1	GND
2	GND
3	RF In
4	GND
5	GND
6	GND
7	GND
8	GND
9	GND
10	GND
11	GND
12	GND
13	RF Out
14	GND
15	GND
16	GND
17	VD
18	GND
19	GND
20	GND

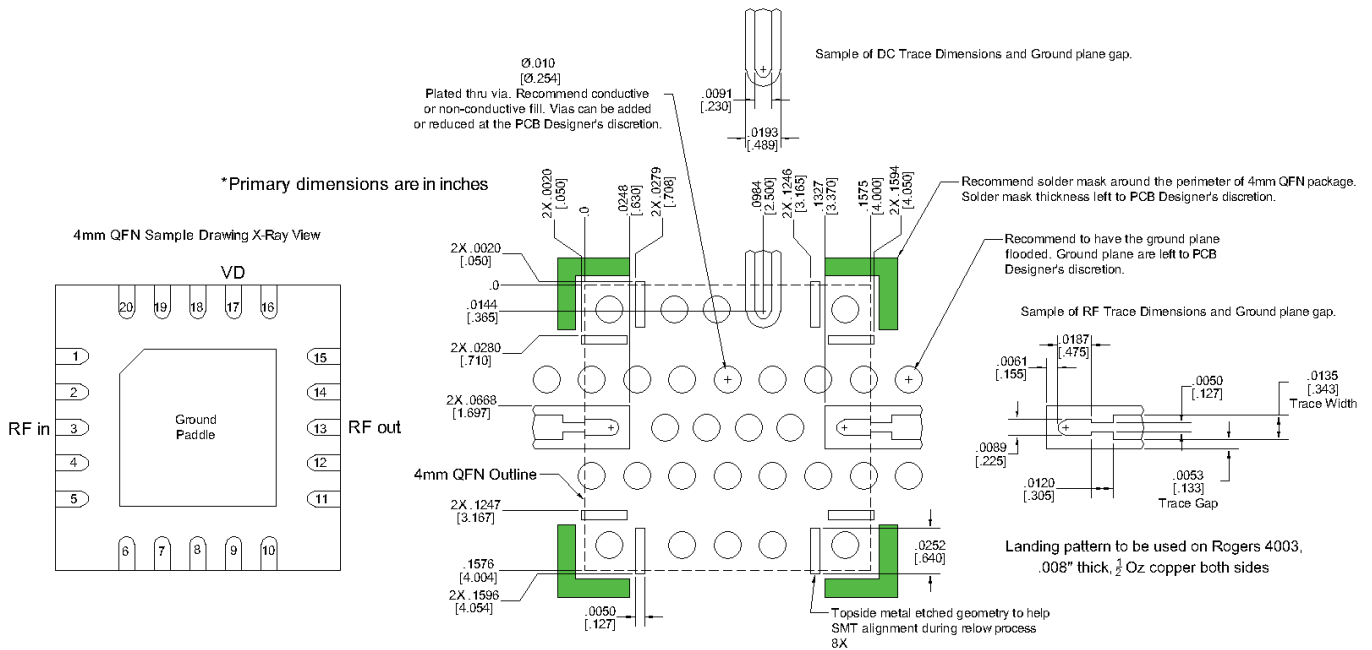
Notes (unless otherwise specified):

- Substrate material is LCP.
- I/O Leads and Die Paddle is (from base to finish):
 Ni: 0.5 - 2.0 um
 Pd: 0.08 - 0.15 um
 Au: 0.003 um Min.
- All unconnected pins should be connected to PCB RF ground.

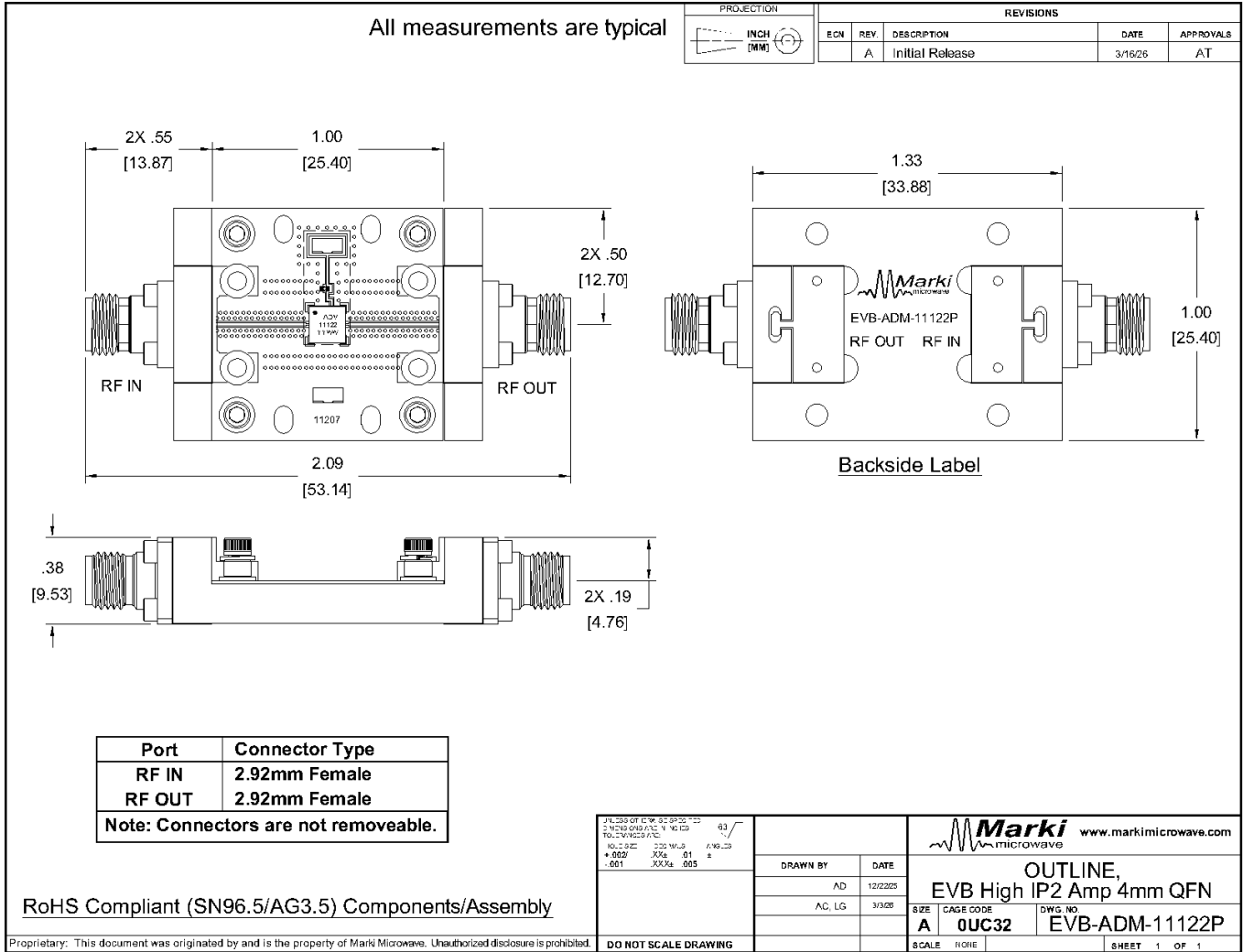
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES AND DECIMAL FRACTIONS TOLERANCES ARE: FRACTIONS DECIMALS MILLIMETERS +.002 / -.001 .005 .01 .05	NOTES: DRAWN BY: Tmn DATE: 01-05-2026 A.C. LG 3/3/26	 www.markimicrowave.com Outline 4mm QFN Amplifier CAGE CODE: 0UC32 DWG. NO: ADM-11122PSM
Proprietary: This document was originated by and is the property of Marki Microwave. Unauthorized disclosure is prohibited.		SIZE: A DO NOT SCALE DRAWING SHEET 1 OF 1

Footprint Image

Download : [Footprint Drawing](#)



Evaluation Board - Outline Drawing



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