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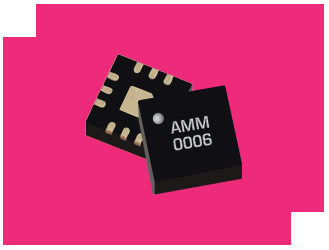
AMM-9852PSM

DC - 20 GHz Wideband Low Noise Amplifier

DEVICE OVERVIEW

General Description

The AMM-9852PSM is a wideband low noise amplifier capable of providing 17dB gain and +33 dBm OIP3 with a low 1.8 dB typical noise figure. The AMM-9852PSM is an ideal linear signal amplifier for applications requiring low power consumption and small form-factors. This amplifier has exceptionally flat response across its entire operating bandwidth.



Download s-parameters here

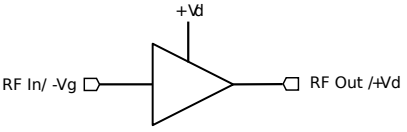
Features

- Broadband DC to 20GHz Operation
- Low Noise Figure
- Exceptionally Flat RF Performance Across Frequency
- Excellent Return Losses

Applications

- Mobile test and measurement equipment
- Radar and satellite communications
- 5G transceivers
- LO driver for Marki L-, H-, and S-diode mixers

Functional Block Diagram



Part Ordering Options

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
AMM-9852PSM	DC - 20 GHz Wideband Low Noise Amplifier	QFN	REACH RoHS	Released	EAR99
EVB-AMM-9852P-1	Evaluation Board, DC-20GHz GaAs Surface Mount Driver Amplifier	EVB	RoHS	Released	EAR99
EVB-AMM-9852P-2	Evaluation Board, DC-20GHz GaAs Surface Mount Driver Amplifier	EVB	RoHS	Released	EAR99

Table Of Contents

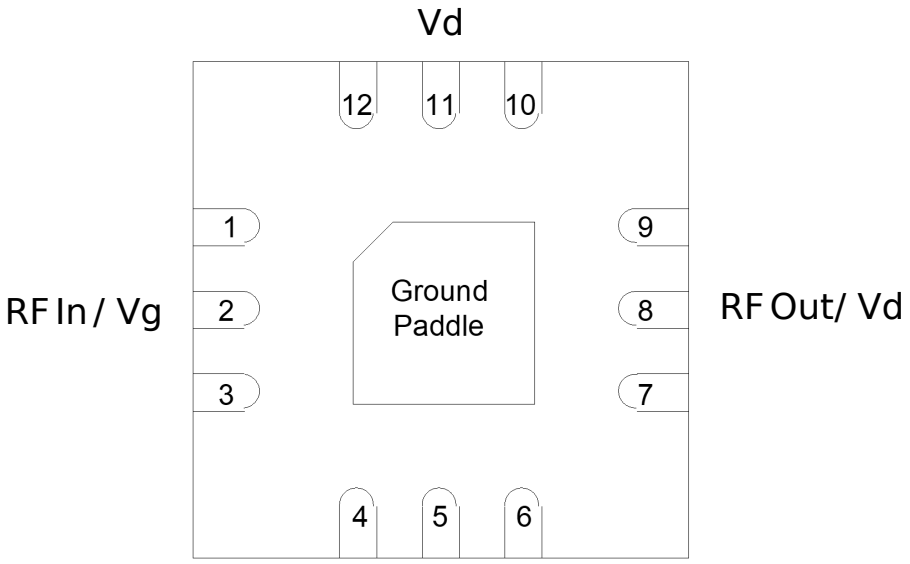
Revision History

Revision Code	Revision Date	Comment
-	2025-03-10	Initial Release
A	2025-08-04	Positive Drain Supply Current Maximum Updated
B	2026-02-13	MTTF Table Added.

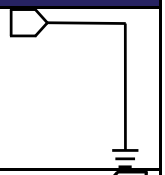
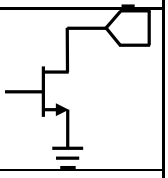
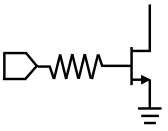
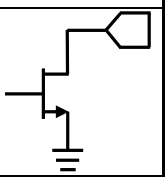
Port Configuration and Functions

Port Diagram

A port diagram of the AMM-9852PSM's QFN package is shown below. The diagram is shown as a top down x-ray view.



Port Functions

Port	Function	Description	DC Equivalent Circuit
GND	Ground	Ground paddle and non-connected pins must be connected to a DC/RF ground potential with high thermal and electrical conductivity, and low inductance.	
Pin 11	Vd	Pin 11 is the DC bias supply for the amplifier. This pin should be connected to the same supply voltage being used to supply the pin 8 "RF Out / Vd" bias-tee.	
Pin 2	RF In / Vg	Pin 2 is the RF input of the amplifier and also provides DC bias to the amplifier. This input in internally RF matched to 50 Ohms and requires a bias-tee to a negative DC bias voltage. The bias voltage applied to this pin directly controls the drain current (Id into pin 8) of the amplifier. As the voltage on this pin becomes more negative, drain current decreases. Voltage should be applied to pin 2 before pin 11 "Vd" and pin 8 "RF Out/Vd". See the section on Sequencing Requirements for more details. Current Ig will flow out of this port. The -Vg supply should be capable of sinking current up to 30mA.	
Pin 8	RF Out / Vd	Pin 8 is the RF output and primary DC power supply of the amplifier. This pin is internally RF matched to 50 ohms and requires an external bias-tee connected to a positive DC supply voltage. Voltage should be applied to pin 2 "RF In/Vg" before applying voltage to pin 8 and pin 11. See the section on Sequencing Requirements for more details.	
		These pins are not internally connected to the amplifier die. It is	

Specifications

Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If these limits are exceeded, the device may be inoperable or have a reduced lifetime. This amplifier is designed and characterized in a 50Ω system, and operation in a reflective environment can cause performance degradation.

Parameter	Maximum Rating	Unit
Maximum Drain-to-Gate Voltage Differential (Vd-Vg)	6.7	V
Maximum Operating Temperature	85	°C
Maximum Storage Temperature	150	°C
Max Junction Temperature for MTTF > 1E6 hours	175	°C
Minimum Operating Temperature	-40	°C
Minimum Storage Temperature	-65	°C
Negative Bias Voltage (Pin 2)	-2	V
Positive Drain Supply Current (with RF Input)	100	mA
Positive Drain Supply Voltage (Pin 8, 11)	8	V
RF Input Power	10	dBm
Thermal Resistance, θJC	120	°C/W

FIT and MTTF Table

T (°C)	λ (TIF)	MTTF (hr)	MTTF (yr)
105	2,441.45	4.10E+05	47
85	310.48	3.22E+06	368
55	8.79	1.14E+08	12,992
25	0.12	8.24E+09	941,063

Package Information

Parameter	Details	Rating
Dimensions	-	3 x 3 mm
Moisture Sensitivity Level	-	MSL 1

Recommended Operating Conditions

The Recommended Operating Conditions indicate the limits, inside which the device should be operated, to guarantee the performance given in Electrical Specifications. Operating outside these limits may not necessarily cause damage to the device, but the performance may degrade outside the limits of the Electrical Specifications. For limits, above which damage may occur, see Absolute Maximum Ratings .

Parameter	Min	Nominal	Max	Unit
Gate Bias DC Voltage	-0.4	-0.2	-0.2	V
Power Supply DC Voltage	5	5	5	V
Ambient Temperature	-40	25	85	°C
Gate DC Current (Ig)	-11.8	-11	-11	mA
Positive DC Current (Id) (No RF Input)	48	89	89	mA

Sequencing Requirements

Turn-on Procedure:
1. Apply Vg (Pin 2)
2. Apply Vd (Pin 8, 11)

Turn-off Procedure:
1. Turn off Vd (Pin 8, 11)
2. Turn off Vg (Pin 2)

Note: RF input power can be injected at any moment in the bias sequencing procedure.

Electrical Specifications

The electrical specifications apply at TA=+25°C in a 50Ω system. QFNs are 100% RF tested.

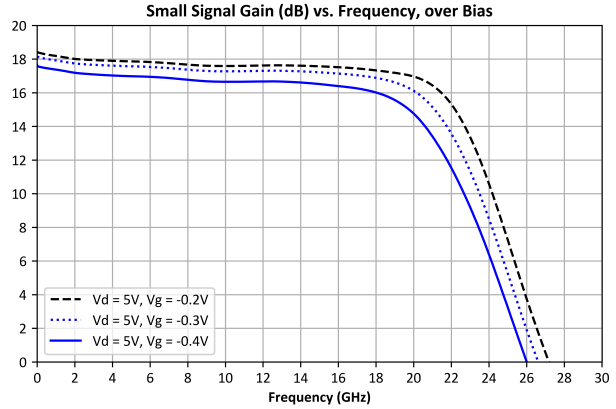
Parameter	Test Conditions	Minimum Frequency (GHz)	Maximum Frequency (GHz)	Min	Typ	Max	Unit
Saturated Output Power	-	2	15	-	21	-	dBm
Saturated Output Power	-	2	20	-	19	-	dBm
Current Consumption [1]	5V/-0.2V bias	-	-	-	89	-	mA
Gate Current, Ig [2]	5V/-0.2V bias	-	-	-	-11	-	mA
Input Return Loss	5V/-0.2V bias, -20 dBm Input Power	0	20	-	18	-	dB
Noise Figure	5V/-0.2V bias, -20 dBm Input Power	0	20	-	1.8	-	dB
Output IP3	5V/-0.2V bias, -20 dBm Input Power	0	20	-	33	-	dBm
Output P1dB	5V/-0.2V bias	0	12	-	20	-	dBm
Output P1dB	5V/-0.2V bias	12	20	-	16	-	dBm
Output Return Loss	5V/-0.2V bias, -20 dBm Input Power	0	20	-	18	-	dB
Reverse Isolation	5V/-0.2V bias, -20 dBm Input Power	0	20	-	21	-	dB
Small Signal Gain	5V/-0.2V bias, -20 dBm Input Power	0	20	-	17.5	-	dB

[1] Bias conditions for Id tested with no RF input power. Bias conditions presented as Vd/Vg.
[2] Gate current Ig is shown as a negative value representing it's direction of flow out of Pin 2 when -Vg is applied.

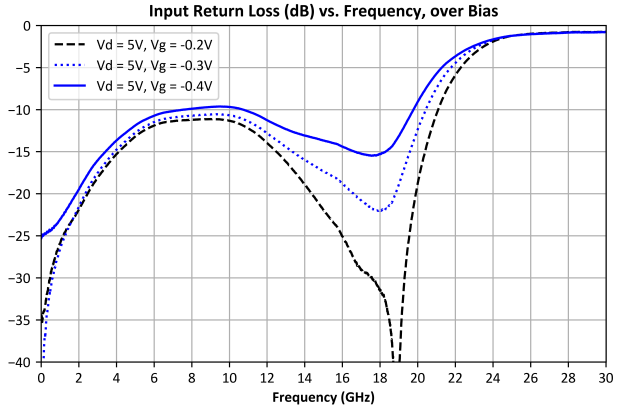
Typical Performance Plots (vs Bias)

Measurement data de-embedded using standard evaluation board and external wideband test equipment bias tees.

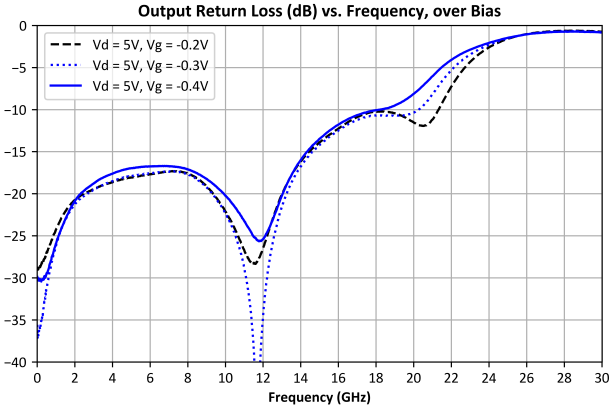
Small Signal Gain (dB) vs. Frequency, over Bias



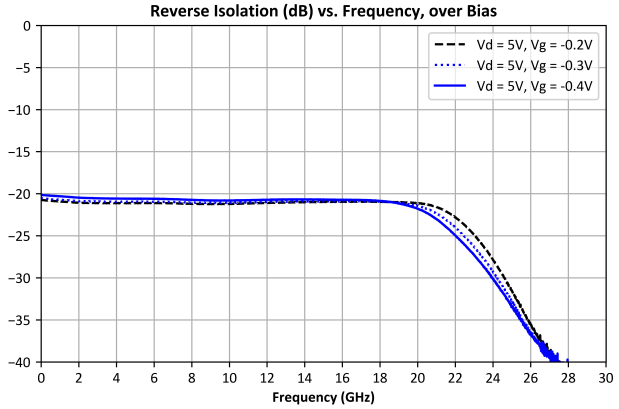
Input Return Loss (dB) vs. Frequency, over Bias



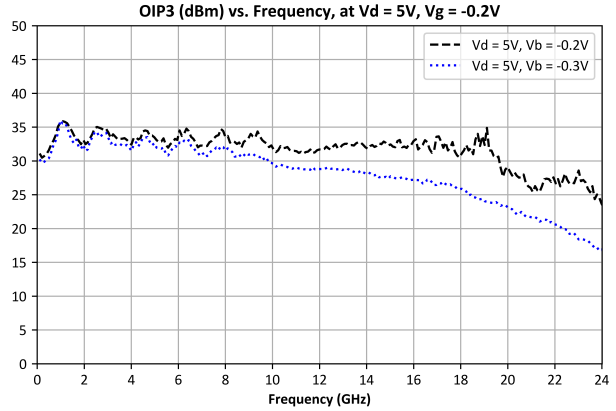
Output Return Loss (dB) vs. Frequency, over Bias



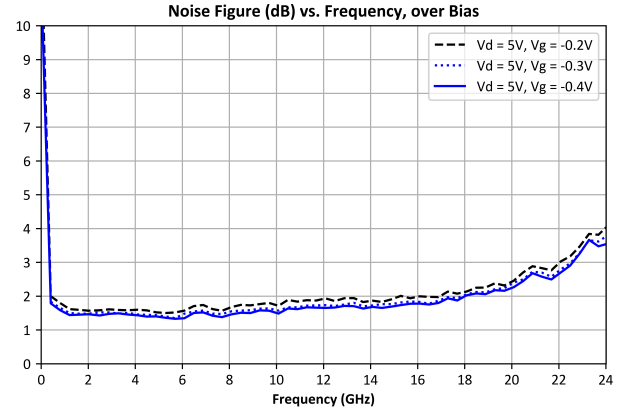
Reverse Isolation (dB) vs. Frequency, over Bias



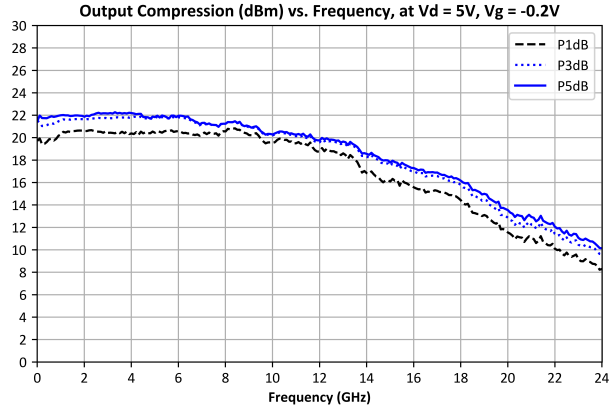
OIP3 (dBm) vs. Frequency, at Vd = 5V, Vg = -0.2V



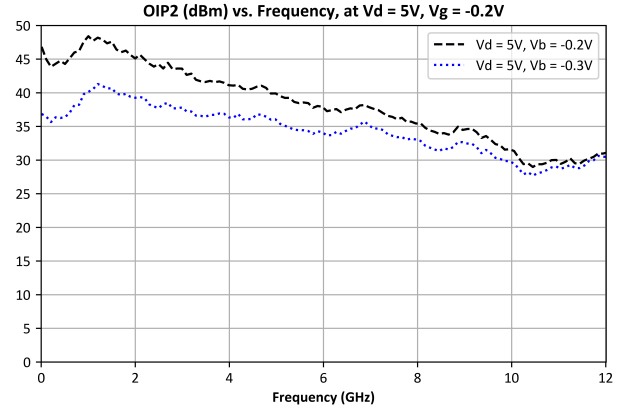
Noise Figure (dB) vs. Frequency, over Bias

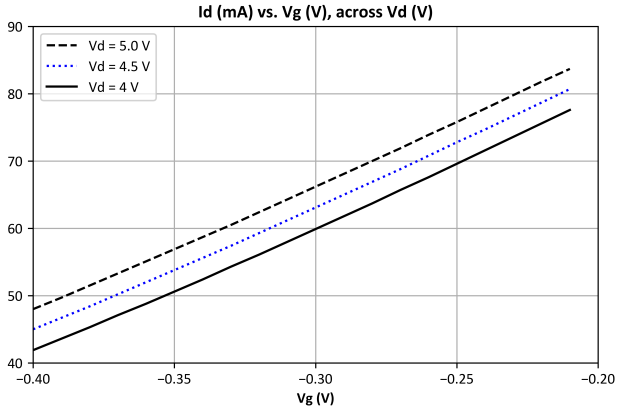


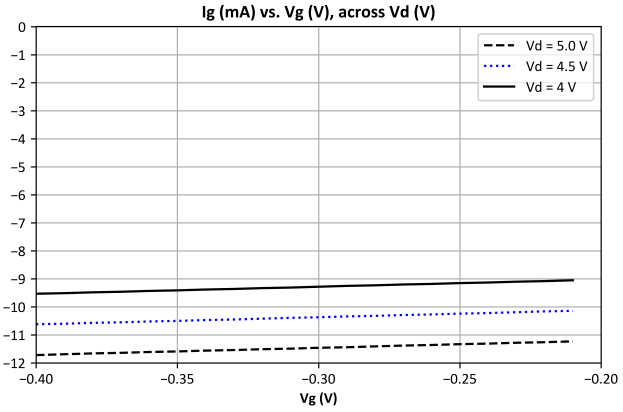
Output Compression (dBm) vs. Frequency, at Vd = 5V, Vg = -0.2V



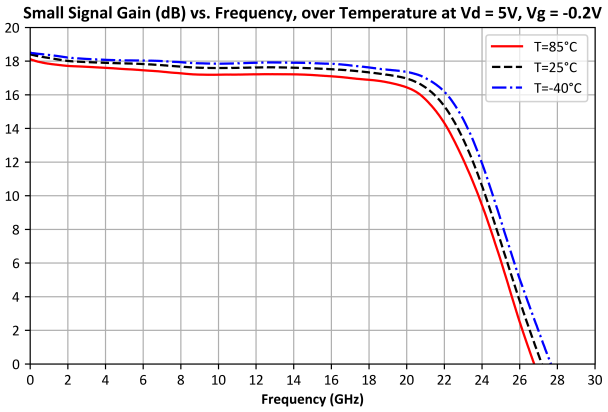
OIP2 (dBm) vs. Frequency, at Vd = 5V, Vg = -0.2V

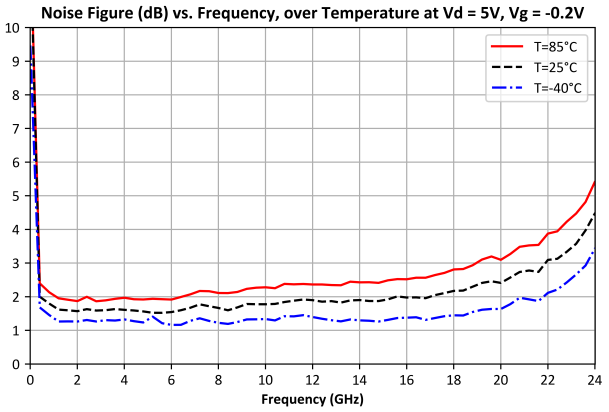




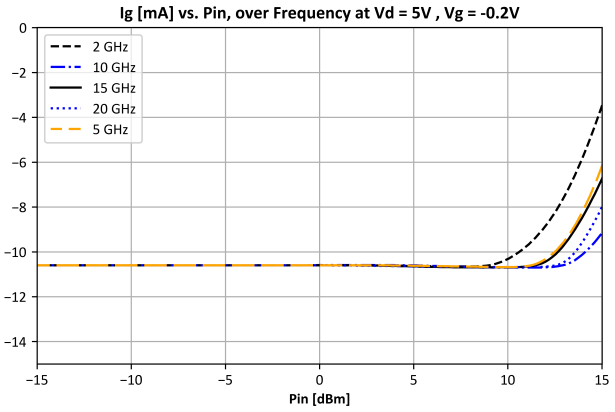


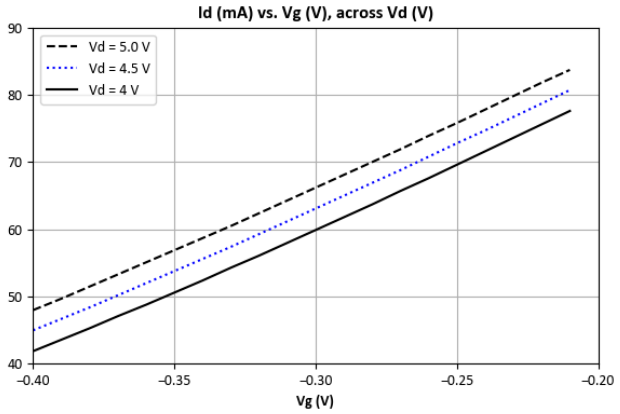
Typical Performance Plots (vs Temperature)

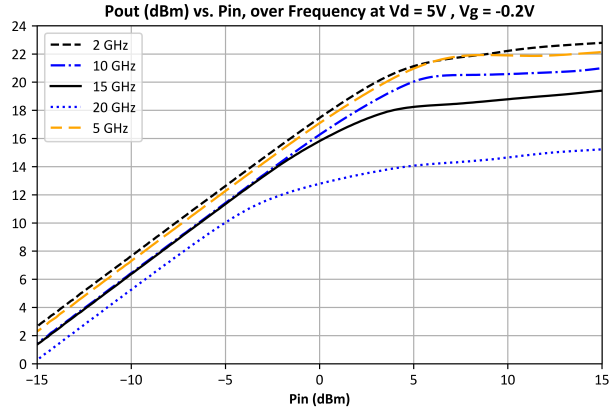


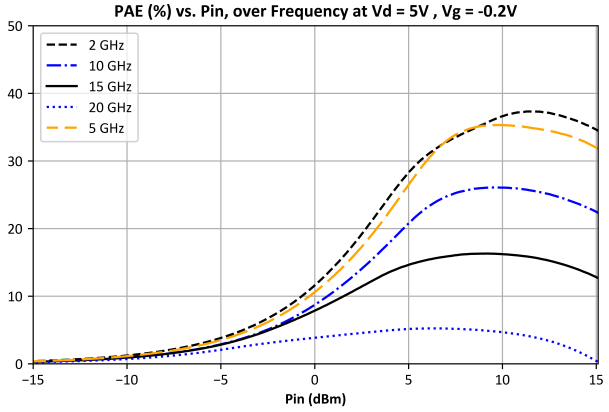


Typical Performance Plots (vs Input Power)





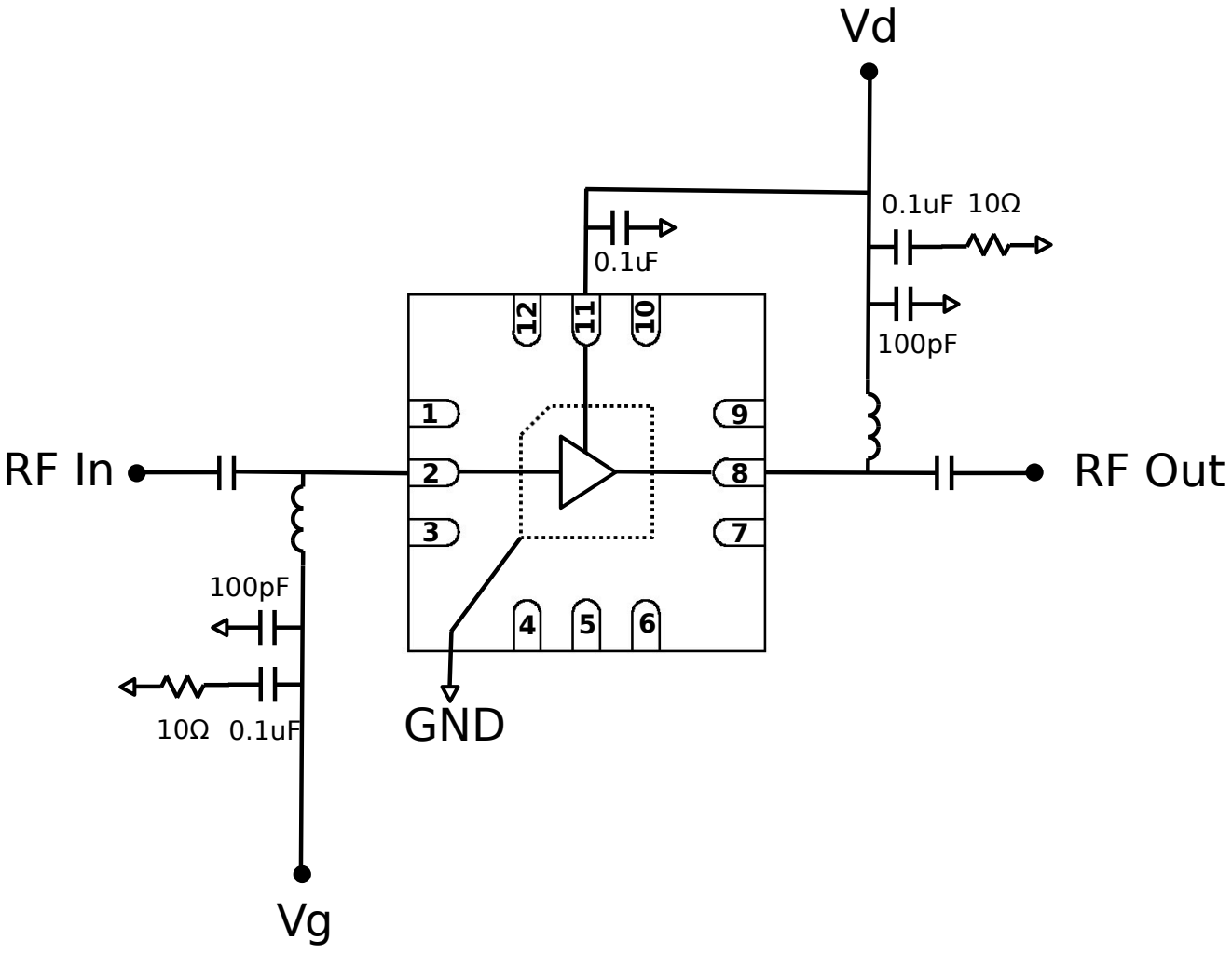




Application Information

Below is the recommended application circuit for the AMM-9852PSM. This is the configuration that is used to characterize this device. However, each PCB layout and environment are different which may require minor modifications of the biasing network. Please contact support@markimicrowave.com for more information.

Application Circuit



Application Circuit Description

The AMM-9852PSM requires biasing through the RF input and output ports as well as the dedicated Vd port. This requires the use of DC blocking capacitors and RF choke inductors at both the input and output. Single placement modular bias tees, such as the Marki BTL-0035SMG-2, could also be used in place of discrete SMD components. It is possible to extend low-frequency performance by using “stacked” choke inductors and sufficiently large DC blocking caps to not impede RF signal at the frequency of interest. The general tradeoff is external parts count vs low frequency performance. Contact Marki technical support if you need assistance with a low-frequency application circuit for this part. Datasheet performance was measured using external wideband test equipment bias tees.

Constant Current and Constant Voltage Operation

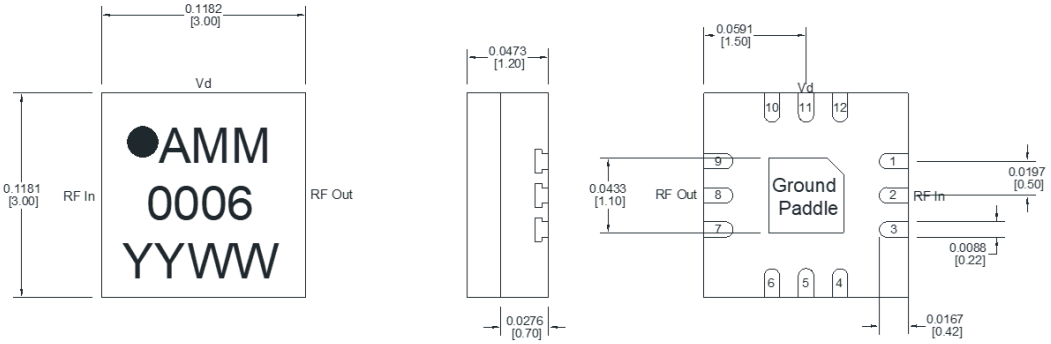
As with most amplifiers utilizing HEMT technology, the AMM-9852PSM can be biased with a constant gate and drain voltage, or with a constant drain current by regulating the gate voltage. Using a constant gate and drain voltage for biasing reduces complexity, but has variable current consumption during operation. On the other hand, biasing the gate using a feedback network that samples the drain current minimizes unit-to-unit variation in gain and other parameters.

Under small signal excitation at a fixed temperature, these two approaches are equivalent. However, they will diverge in large signal conditions, where the drain current is affected by the frequency and power of the input signal. In these conditions P1dB, P3dB, and P5dB will be somewhat different, but based on tests with similar parts, they will be within a few dBm of the constant voltage curves.

Mechanical Data

Outline Drawing

Download : Outline 2D Drawing



PROJECTION
INCH
[MM]

All dimensions are typical

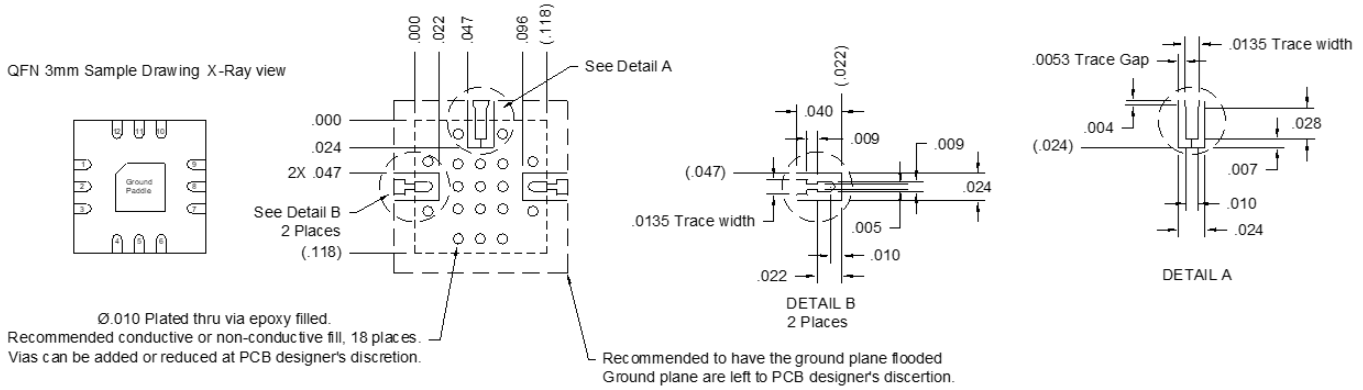
Notes (unless otherwise specified):

1. Substrate material is LCP.
2. I/O Leads and Die Paddle are 0.05 micron Au over 0.02 microns Pd over 0.5 microns Ni.
3. All unconnected pins should be connected to PCB RF ground.

Pad #	Function
1	N/C
2	RF In
3	N/C
4	N/C
5	N/C
6	N/C
7	N/C
8	RF Out
9	N/C
10	N/C
11	Vd
12	N/C

Footprint Image

Download : Footprint Drawing



The landing pattern is to be used on Rogers 4003,
0.008" thick, $\frac{1}{2}$ Oz Cu.

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