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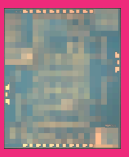
AMM-9893CH

45-95GHz mmWave LO Driver Amplifier

DEVICE OVERVIEW

General Description

The AMM-9893CH is a wideband mmWave amplifier enabling operation over a 45-95 GHz bandwidth. The amplifier features 18dB gain, excellent return losses, and 18dBm output power. Available as a wire-bondable die, or packaged in a connectorized module under the part number AMM-9893M



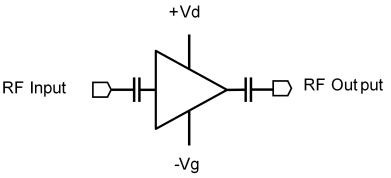
Features

- Ultra-broadband operation (45-95GHz)
- 18dB gain
- Excellent return losses

Applications

- Test and Measurement Equipment
- SATCOM
- LO signal chain for mmWave mixers
- Radar
- Electronic warfare equipment
- Aerospace and Defense

Functional Block Diagram



Part Ordering Options

Part Number	Description	Package	Connectors	Green Status	Product Lifecycle	Export Classification
AMM-9893M	45 – 95 GHz mmWave LO Driver Amplifier	M	-	REACH RoHS	Released	3A001.b.4.e.3
AMM-9893CH	45-95GHz mmWave LO Driver Amplifier	CH	-	REACH RoHS	Released	3A001.b.2.h

Table Of Contents

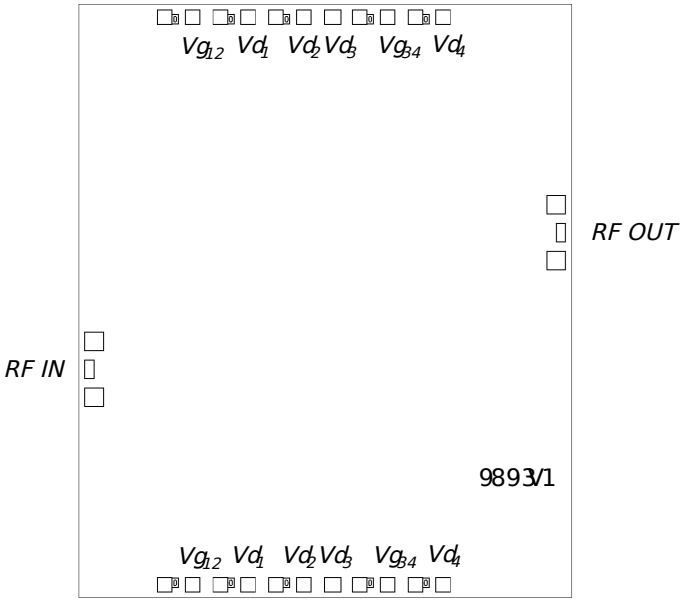
Revision History

Revision Code	Revision Date	Comment
-	2024-10-09	Initial Release
A	2026-02-13	MTTF Table Added.

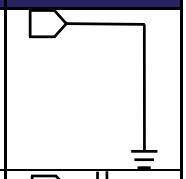
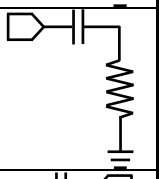
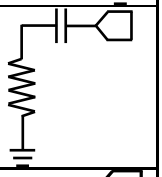
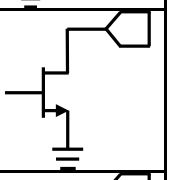
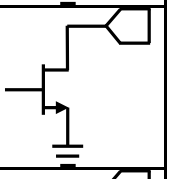
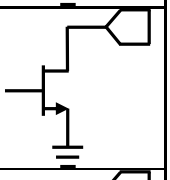
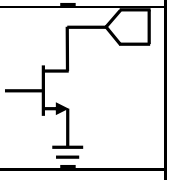
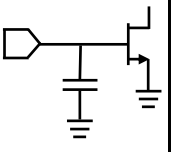
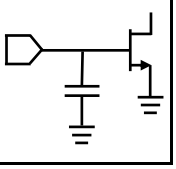
Port Configuration and Functions

Port Diagram

The port diagram of the AMM-9893CH is shown below. There are two sets of DC pads, one on the North and one on the South edge of the die. They perform identical functions and are internally connected on the die. They are provided for convenience in bias routing and only one pad of each type needs to be connected.



Port Functions

Port	Function	Description	DC Equivalent Circuit
GND	Ground	Bottom side of the die must be connected to a DC/RF ground with high thermal and electrical conductivity. There is no need to bond to the Gnd pads on the top of the die.	
RF In	RF Input	The amplifier's RF Input pad, this pad has an internal DC blocking capacitor and is RF matched to 50 Ohms.	
RF Out	RF Output	The amplifier's RF Output pad, this pad has an internal DC blocking capacitor and is RF matched to 50 Ohms.	
VD1	Positive DC Supply Voltage	This pad provides DC power to the drain of the first stage of the amplifier. DC voltage at this pin should be set to 3.5V for normal operation.	
VD2	Positive DC Supply Voltage	This pad provides DC power to the drain of the second stage of the amplifier. DC voltage at this pin should be set to 3.5V for normal operation.	
VD3	Positive DC Supply Voltage	This pad provides DC power to the drain of the third stage of the amplifier. DC voltage at this pin should be set to 3.5V for normal operation.	
VD4	Positive DC Supply Voltage	This pad provides DC power to the drain of the fourth stage of the amplifier. DC voltage at this pin should be set to 3.5V for normal operation.	
VG12	Gate Bias Voltage	This pad provides DC bias to the gates of stages 1 and 2 of the amplifier. This pin requires a negative bias voltage for normal operation. The drain current Id of the amplifier will be controlled by the voltage applied to this pin. As this voltage becomes more positive, drain current will increase. For normal operation, the voltage on this pin should be the same as Vg34 and set to produce a drain current of 350mA.	
VG34	Gate Bias Voltage	This pad provides DC bias to the gates of stages 3 and 4 of the amplifier. This pin requires a negative bias voltage for normal operation. The drain current Id of the amplifier will be controlled by the voltage applied to this pin. As this voltage becomes more positive, drain current will increase. For normal operation, the voltage on this pin should be the same as Vg12 and set to produce a drain current of 350mA.	

Specifications

Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If these limits are exceeded, the device may become inoperable or have a reduced lifetime. Reliability limits are individual, instantaneous catastrophic limits only. Functional operation limits are indicated below. Operation of the device at multiple absolute maximum limits or for extended periods at a single limit can cause degradation and damage to the device.

Parameter	Maximum Rating	Unit
Drain Supply Voltage (Vd)	4	V
Gate Supply Voltage (Vg)	-1.5	V
Maximum Operating Temperature for MTTF > 1E6 hours	85	°C
Maximum Storage Temperature	125	°C
Minimum Operating Temperature for MTTF > 1E6 hours	-40	°C
Minimum Storage Temperature	-65	°C
Positive Drain Supply Current (Id) (with RF Input)	450	mA
RF Input Power	15	dBm

FIT and MTTF Table

T (°C)	λ (TIF)	MTTF (hr)	MTTF (yr)
105	2,441.45	4.10E+05	47
85	310.48	3.22E+06	368
55	8.79	1.14E+08	12,992
25	0.12	8.24E+09	941,063

Package Information

Parameter	Details	Rating
Dimensions	-	2.652 x 3.192

Recommended Operating Conditions

The Recommended Operating Conditions indicate the limits, inside which the device should be operated, to guarantee the performance given in Electrical Specifications. Operating outside these limits may not necessarily cause damage to the device, but the performance may degrade outside the limits of the Electrical Specifications. For limits, above which damage may occur, see Absolute Maximum Ratings.

Parameter	Min	Nominal	Max	Unit
Positive DC Voltage (Vd)	-	3.5	-	V
Gate Bias DC Voltage (Vg)	-	2	-	V
Positive DC Current (Id) (No RF Input) [1]	-	350	-	mA
Input Power for Saturation	-	5	-	-

[1] Recommended operating current condition without RF input applied.

Sequencing Requirements

Turn-on Procedure:
1: Apply Vg = -1.5V (VGG2 pad)
2: Apply Vd voltage (VDD/ACG2 pad)
3: Increase Vg voltage towards -0.2V to achieve Id=350mA.
4: Apply RF input Power
Turn-off Procedure:
1: Turn off RF input Power
2: Turn off Vd voltage (VDD/ACG2 pad)
3: Turn off Vg voltage (VGG2 pad)

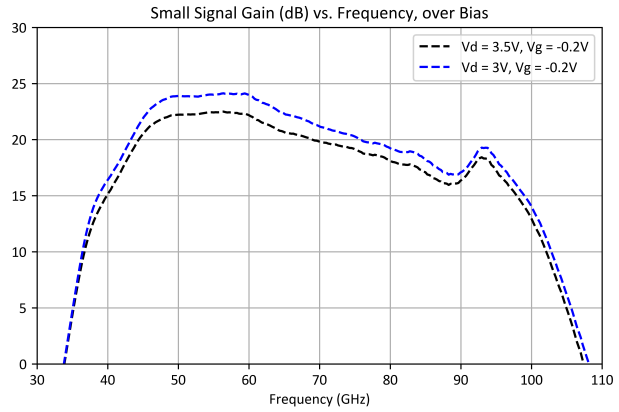
Electrical Specifications

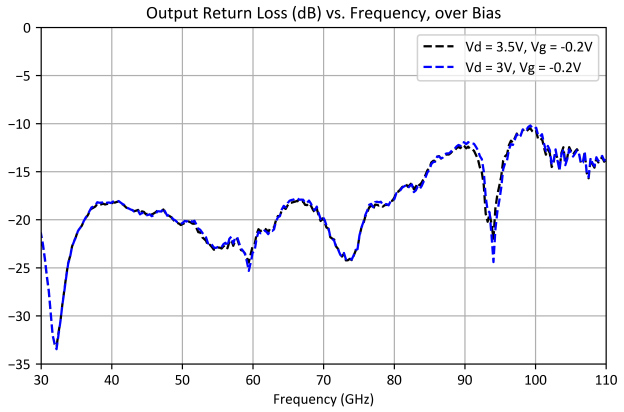
Unless otherwise specified, electrical specifications apply at TA=+25°C, Vd = 5V and Vg set such that Id = 350mA.

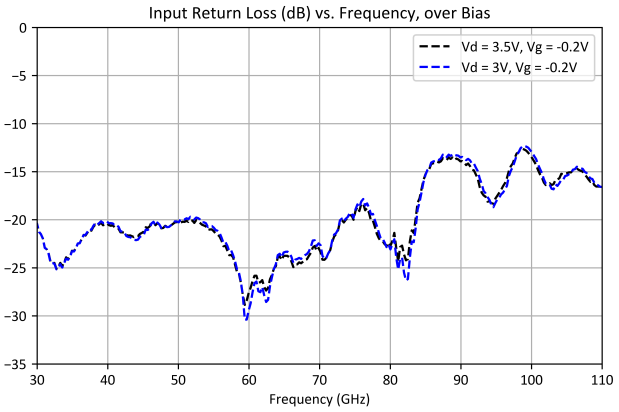
Parameter	Test Conditions	Minimum Frequency (GHz)	Maximum Frequency (GHz)	Min	Typ	Max	Unit
Input Return Loss	Vd=3.5V, Vg=-0.2V Pin=-20dBm	45	95	-	15	-	dB
Output Return Loss	Vd=3.5V, Vg=-0.2V Pin=-20dBm	45	95	-	15	-	dB
Saturated Output Power	Vd=3.5V, Vg=-0.2V	45	95	-	18	-	dBm
Small Signal Gain	Vd=3.5V, Vg=-0.2V Pin=-20dBm	45	95	-	18	-	dB

Performance plots measured using the recommended application circuit shown below.

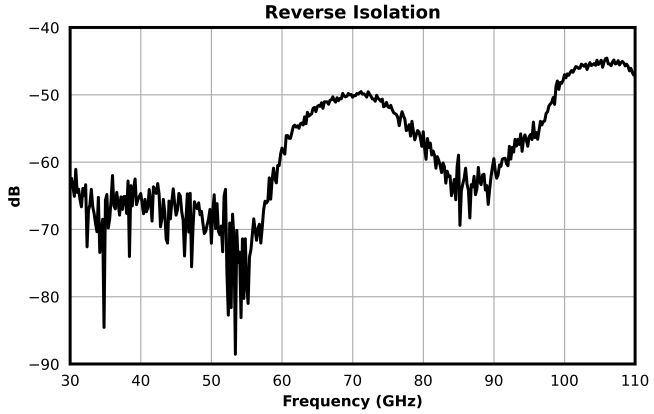
Typical Performance Plots

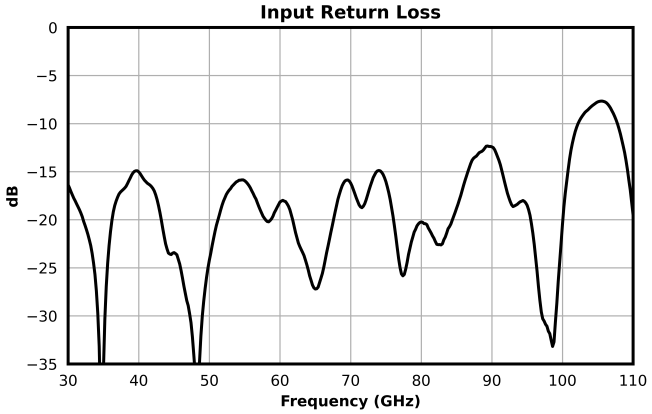


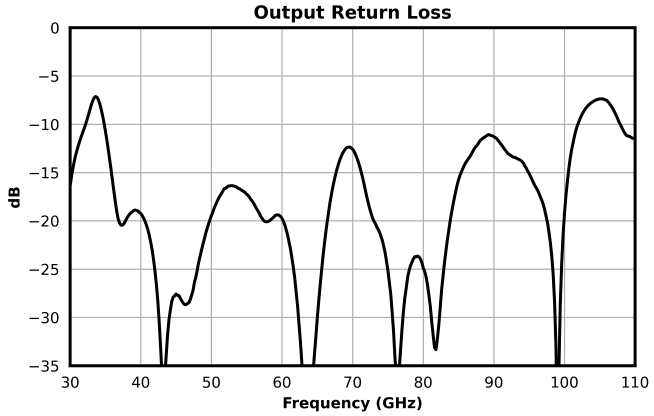


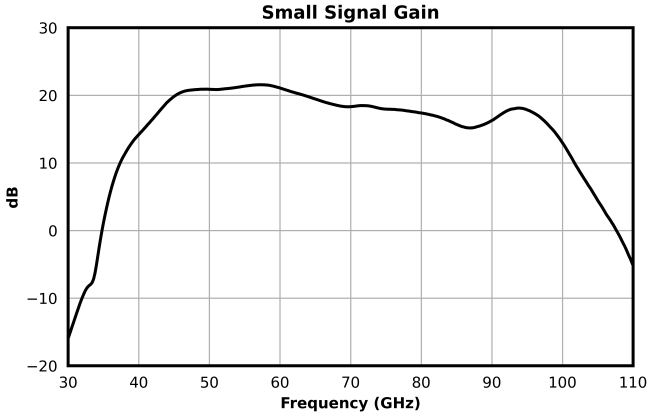


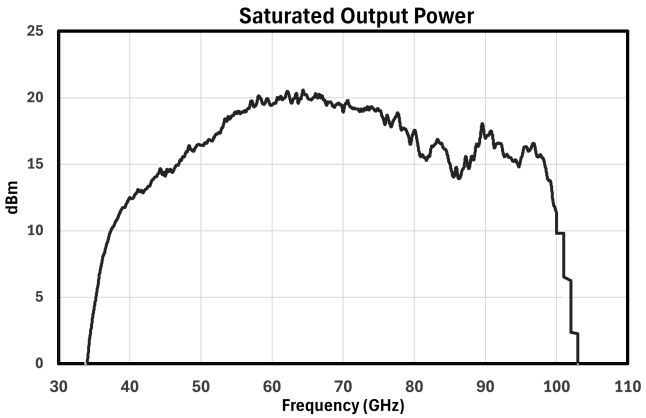
Typical Performance Plots (AMM-9893M Module)





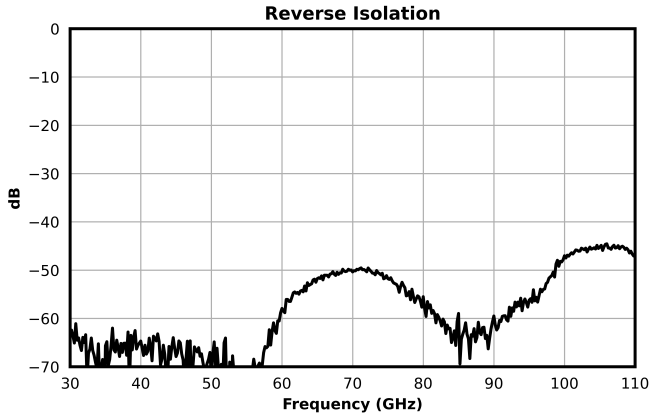


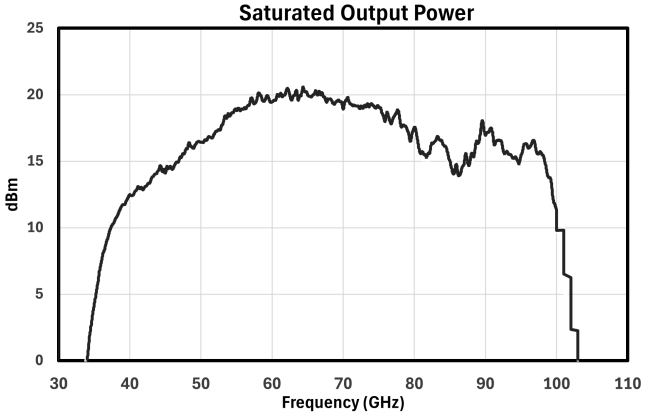


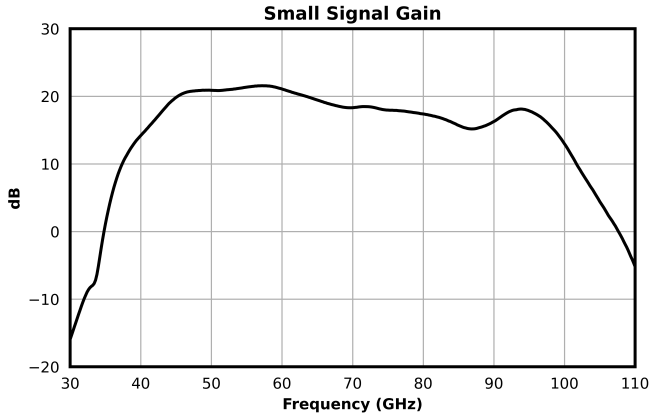


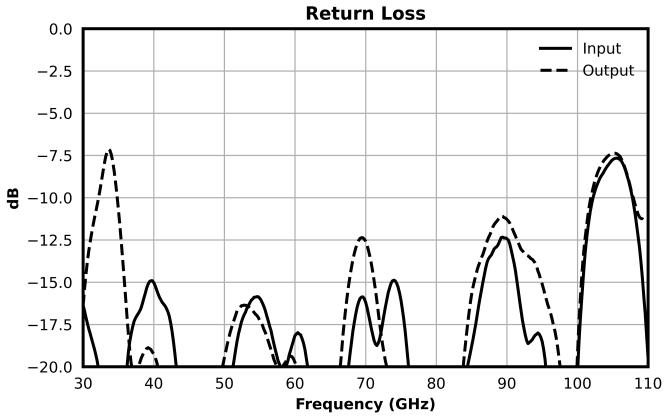
AMM-9893M - Typical Performance Plots

Performance plots for the connectorized module are shown for measurements where directly probed measurements of the die are unavailable. Note that the following measurements include losses from connectors and microstrip traces.

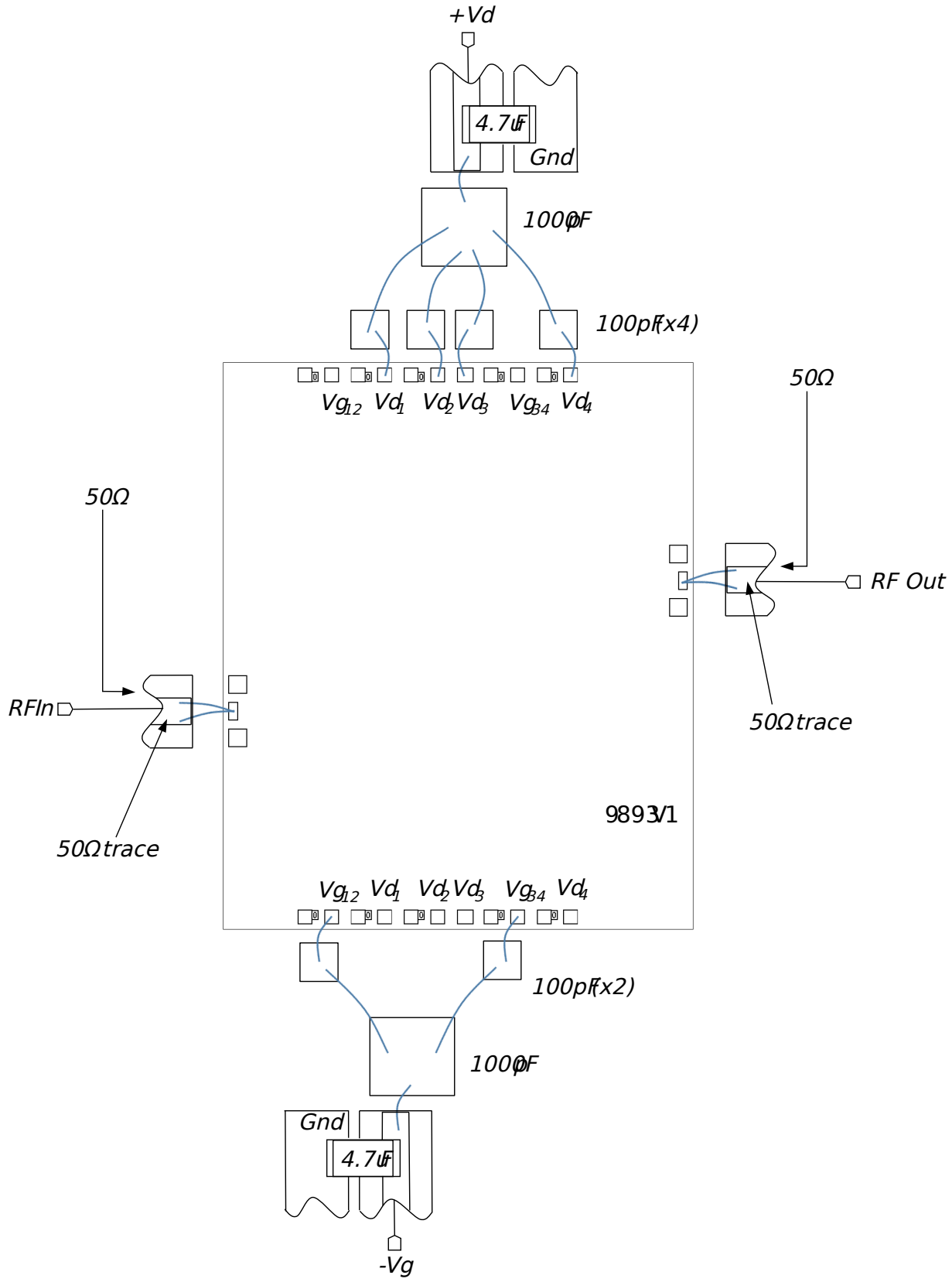








Application Circuit



Application Circuit Description

Above is the recommended application circuit for the AMM-9893CH. Multiple DC power supply bypassing capacitors are shown around the die. These capacitors are of the vertical wire-bondable type. The smaller capacitors are100pF and the larger capacitors are 1000pF. In addition to the wire-bondable capacitors, 4.7uF SMD capacitors are recommended at the +Vd and -Vg inputs.

DC drain voltage is supplied to the amplifier across single 4.7uF and 1000pF bypass capacitors and then individual 100pF bypass capacitors to the Vd1, Vd2, Vd3 and Vd4 pads.

In a similar way, DC gate bias voltage is supplied to the VG12 and VG34 pads across single 4.7uF and 1000pF bypass capacitors and individual 100pF bypass capacitors. 50 Ohm RF input and output traces should be bonded to the AMM-9893CH using "V" bonds as shown in the diagram. DC blocking capacitors are not required at the input and output RF ports of the amplifier.

Note that top and bottom row DC IO pads are identical and are internally connected on the die. This is done to allow flexibility in routing bias voltages to the part. It is only required to attach one of each type of bias pad. For instance if the top row Vd1 pad is connected, the bottom row Vd1 pad can be left floating.

Die Mounting Recommendations

Mounting and Bonding Recommendations

Marki MMICs should be attached directly to a ground plane with conductive epoxy. The ground plane electrical impedance should be as low as practically possible. This willprevent resonances and permit the best possible electrical performance. Datasheetperformance is only guaranteed in an environment with a low electrical impedance ground.

Mounting - To epoxy the chip, apply a minimum amount of conductive epoxy to themounting surface so that a thin epoxy fillet is observed around the perimeter of the chip.Cure epoxy according to manufacturer instructions.

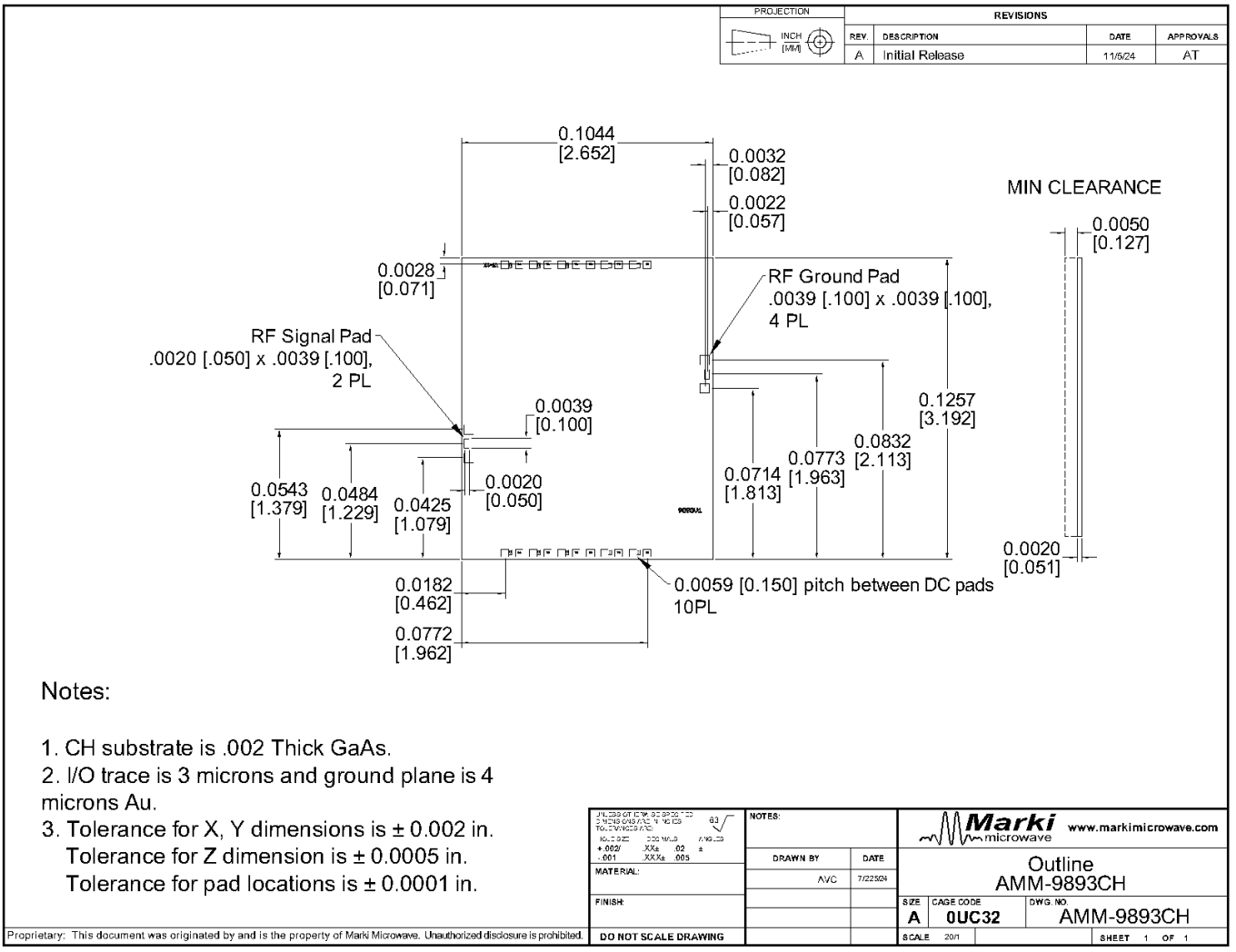
Wire Bonding - Ball or wedge bond with 0.025 mm (1 mil) diameter pure gold wire.Thermosonic wirebonding with a nominal stage temperature of 150 °C and a ball bondingforce of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Usethe minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should bestarted on the chip and terminated on the package or substrate. Bond wire inductancewill improve return loss. Bondwire inductance in the range of 30pH to 200pH will improveperformance.

Circuit Considerations – 50 Ω transmission lines should be used for all high frequencyconnections in and out of the chip. Wirebonds should be kept as short as possible, withmultiple wirebonds recommended for higher frequency connections to reduce parasiticinductance. In circumstances where the chip more than .001” thinner than thesubstrate, a heat spreading spacer tab is optional to further reduce bondwire length and parasitic inductance.

Mechanical Data

Outline Drawing

Download : Outline 2D Drawing



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