Sales: 408-778-9952 | General: 408-778-4200 | Fax: 408-778-4300
Sales & Customer Support: sales@markimicrowave.com
Tech Support: support@markimicrowave.com

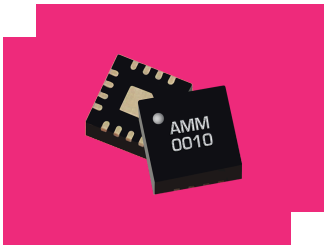
AMM-7199ASM

11-38 GHz GaAs Surface Mount LO Driver Amplifier

DEVICE OVERVIEW

General Description

The AMM-7199ASM is a surface-mount amplifier suitable for use as a single tone driver or general-purpose gain block. It can drive an L or H diode mixer from 11 to 38 GHz, or S diode mixer from 16 to 34 GHz. This amplifier also has low current draw under RF drive, exceptionally low input and output reflections, and excellent gain flatness in-band. The AMM-7199ASM is packaged in a compact 3mm QFN for surface mount integration onto printed circuit boards.



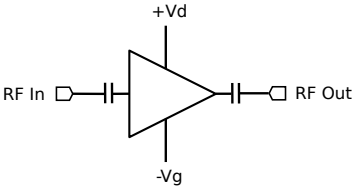
Features

- +21dB Small Signal Gain
- +21 dBm saturated output power
- Excellent return losses
- Compact 3mm QFN package

Applications

- Mobile test and measurement equipment
- Radar
- SATCOM
- LO driver for Marki L-, H-, and S-diode mixers
- 5G transceivers

Functional Block Diagram



Part Ordering Options

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
AMM-7199ASM	11-38 GHz GaAs Surface Mount LO Driver Amplifier	QFN	REACH RoHS	Released	3A001.b.2.d
EVB-AMM-7199ASM	Evaluation Board, 11-38 GHz GaAs Surface Mount LO Driver Amplifier	EVB	REACH RoHS	Released	EAR99

AMM-7199ASM

11-38 GHz GaAs Surface Mount LO Driver Amplifier

Table Of Contents

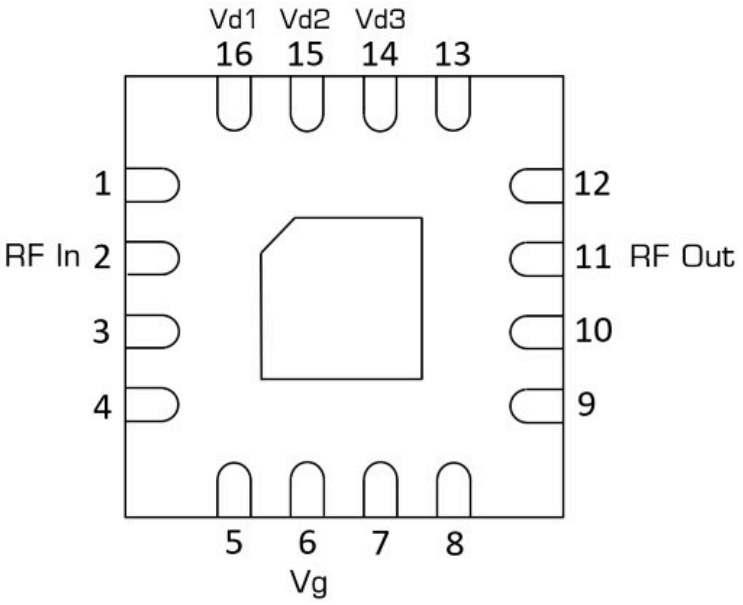
Revision History

Revision Code	Revision Date	Comment
-	2025-12-18	Initial Release

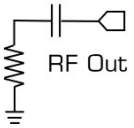
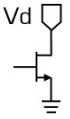
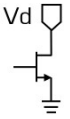
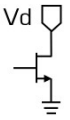
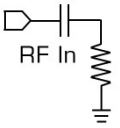
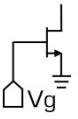
Port Configuration and Functions

Port Diagram

A port diagram of the AMM-7199ASM's QFN package is shown below. The pin functions are detailed in this datasheet.



Port Functions

Port	Function	Description	DC Equivalent Circuit
GND	Ground	Ground paddle and non-connected pins must be connected to a DC/RF ground potential with high thermal and electrical conductivity, and low inductance.	
Pin 11	RF Output	Pin 11 is the RF output of the amplifier, and is matched to 50 ohms. It is internally DC blocked.	
Pin 14	Positive DC Supply Vd	Pins 14 provides +2.5V to +3V DC voltage to the amplifier's third stage. Negative voltage must be supplied to Pin 6 before turning on the positive supply voltage.	
Pin 15	Positive DC Supply Vd	Pins 15 provides +2.5V to +3V DC voltage to the amplifier's second stage. Negative voltage must be supplied to Pin 6 before turning on the positive supply voltage.	
Pin 16	Positive DC Supply Vd	Pins 16 provides +2.5V to +3V DC voltage to the amplifier's first stage. Negative voltage must be supplied to Pin 6 before turning on the positive supply voltage.	
Pin 2	RF Input	Pin 2 is the RF input of the amplifier, and is matched to 50 ohms. It is internally DC blocked.	
Pin 6	Negative DC Supply Vg	Pin 6 provides -0.4V to -0.6V of DC voltage. This must be turned on before turning on the positive supply voltage to Pin 1.	

Specifications

Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If these limits are exceeded, the device may be inoperable or have a reduced lifetime. This amplifier is designed and characterized in a 50Ω system, and operation in a reflective environment can cause performance degradation.

Parameter	Maximum Rating	Unit
Continuous Power Dissipation (PDISS) (at 85 ˚C case temp.) [1]	1	W
Maximum Operating Temperature	85	˚C
Maximum Storage Temperature	150	˚C
Max Junction Temperature for MTTF > 1E6 hours	175	˚C
Minimum Operating Temperature	-40	˚C
Minimum Storage Temperature	-65	˚C
Negative Bias Voltage (Pin 6)	-2	V
Positive Drain Supply Current (with RF Input) [2]	450	mA
Positive Drain Supply Voltage (Pin 14, 15, 16)	4.5	V
RF Input Power	20	dBm
Thermal Resistance, θJC	94	°C/W

[1] Derates by 11 mW/ ˚C above 85 ˚C case temperature.
[2] Positive Drain Supply DC current is specified as Id1 + Id2 + Id3

Package Information

Parameter	Details	Rating
Dimensions	-	3 x 3 mm
Moisture Sensitivity Level	-	MSL 1

Recommended Operating Conditions

The Recommended Operating Conditions indicate the limits, inside which the device should be operated, to guarantee the performance given in Electrical Specifications. Operating outside these limits may not necessarily cause damage to the device, but the performance may degrade outside the limits of the Electrical Specifications. For limits, above which damage may occur, see Absolute Maximum Ratings.

Parameter	Min	Nominal	Max	Unit
Power Supply DC Voltage	2.5	3	3	V
Power Supply DC Current [1]	100	150	180	mA
Ambient Temperature	-40	25	85	˚C
Input Power for Saturation	3	6	8	dBm
Gate Bias DC Voltage	-0.6	-0.5	-0.4	V

[1] Power Supply DC current is specified as Id1 + Id2 + Id3 with no RF Applied

Sequencing Requirements

Turn-on Procedure:
1. Apply Vg (Pin 6)
2. Apply Vd (Pin 14, 15, 16)

Turn-off Procedure:
1. Turn off Vd (Pin 14, 15, 16)
2. Turn off Vg (Pin 6)

Note: RF input power can be injected at any moment in the bias sequencing procedure.

Electrical Specifications

The electrical specifications apply at TA=+25°C in a 50Ω system. QFNs are 100% RF tested. Evaluation board losses are mathematically extracted from Saturated output power, Small signal gain, and Noise figure specifications.

Parameter	Test Conditions	Minimum Frequency (GHz)	Maximum Frequency (GHz)	Min	Typ	Max	Unit
Drain Current, Id [1]	3V/-0.4V	-	-	-	180	-	mA
Drain Current, Id [2]	3V/-0.5V	-	-	-	150	-	mA
Drain Current, Id [3]	3V/-0.6V	-	-	-	130	-	mA
Input IP3	3V/-0.5V bias, -20 dBm Input Power	11	38	-	12	-	dBm
Input Power for Saturation	3V/-0.5V bias	11	38	-	6	-	dBm
Input Return Loss	3V/-0.5V bias, -25 dBm Input Power	11	38	-	16	-	dB
Noise Figure	3V/-0.5V Bias	11	38	-	5	-	dB
Output IP3	3V/-0.5V bias, -20 dBm Input Power	11	38	-	29	-	dBm
Output P1dB	3V/-0.5V bias	11	38	-	19	-	dBm
Output Return Loss	3V/-0.5V bias, -25 dBm Input Power	11	38	-	13	-	dB
Reverse Isolation	3V/-0.5V bias, -25 dBm Input Power	11	38	-	53	-	dB
Saturated Output Power [4]	3V/-0.5V bias	15	30	-	21	-	dBm
Saturated Output Power [5]	3V/-0.5V bias	11	15	-	19	-	dBm
Saturated Output Power [6]	3V/-0.5V bias	30	38	-	19	-	dBm
Small Signal Gain	3V/-0.5V bias, -25 dBm Input Power	15	30	-	21	-	dB
Small Signal Gain	3V/-0.5V bias, -25 dBm Input Power	30	38	-	17	-	dB
Small Signal Gain	3V/-0.5V bias, -25 dBm Input Power	11	15	-	20	-	dB

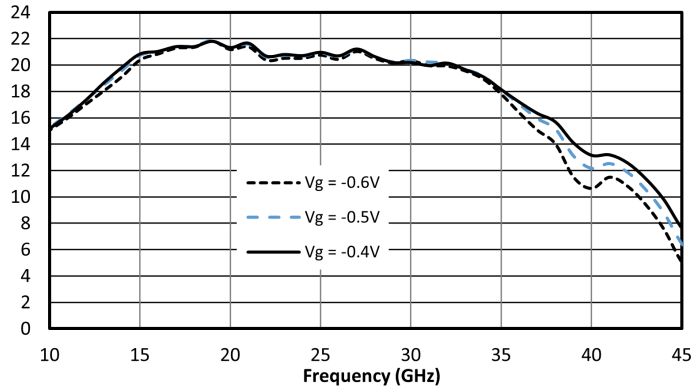
[1][2][3] Bias conditions for Id tested with no RF input power. See Typical Performance Plots for DC current vs. RF power. Bias conditions presented as Vd/Vg. Drain current is specified as Id1 + Id2 + Id3.
[4][5][6] Saturated output power specification defined using the EVB-APM-7199ASM P5dB compression curve shown in Typical Performance Plots, with board losses mathematically extracted.

Typical Performance Plots

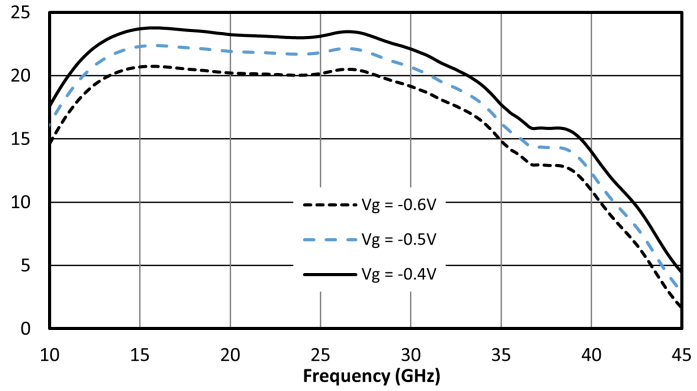
Measurement data taken using the EVB-AMM-7199ASM module.

Evaluation board losses are mathematically extracted out of Output Compression Curves, Small Signal Gain Plots, and Noise Figure plots. All other plots include evaluation board losses.

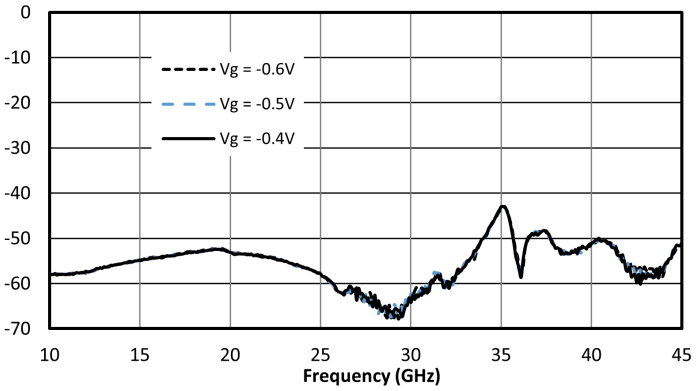
PSat (dBm) vs Frequency, Vd = +3V



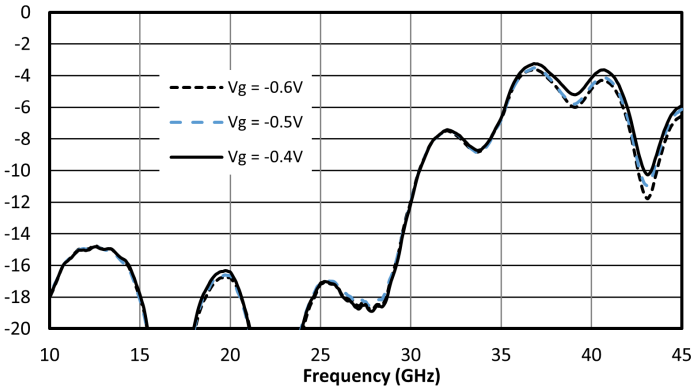
Small Signal Gain (dB) vs Frequency, Vd = +3V



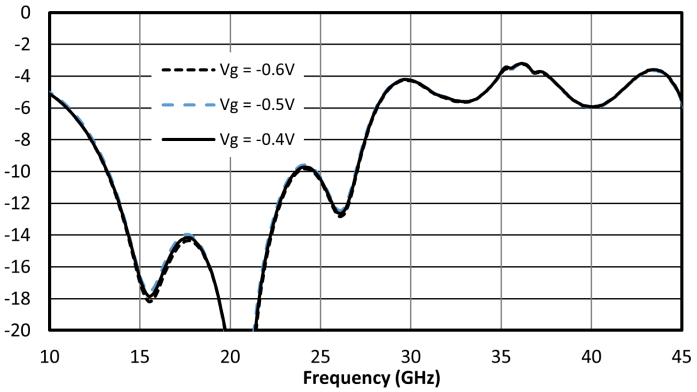
Reverse Isolation (dB) vs Frequency, Vd = +3V



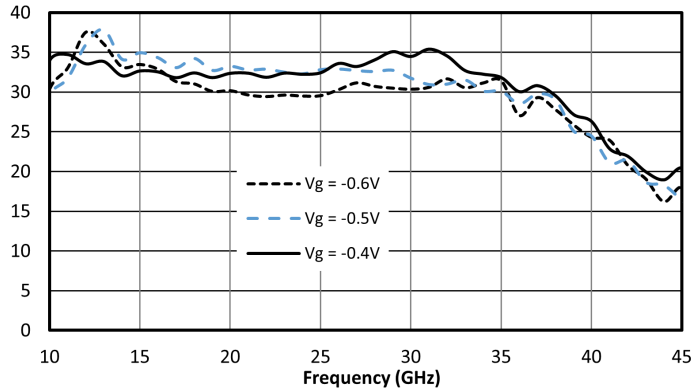
Input Return Loss (dB) vs Frequency, Vd = +3V



Output Return Loss (dB) vs Frequency, Vd = +3V



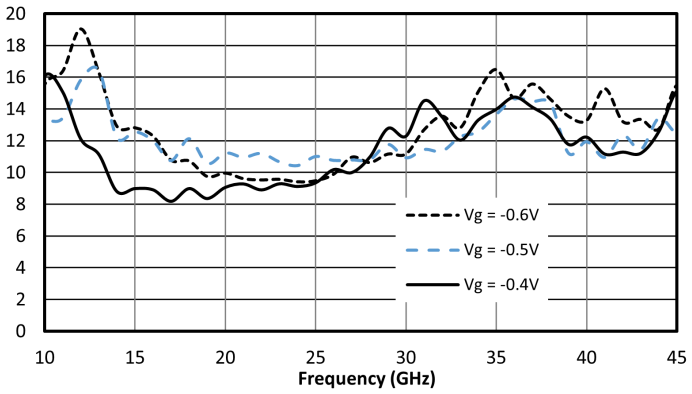
OIP3 (dBm) vs Frequency, Vd = +3V



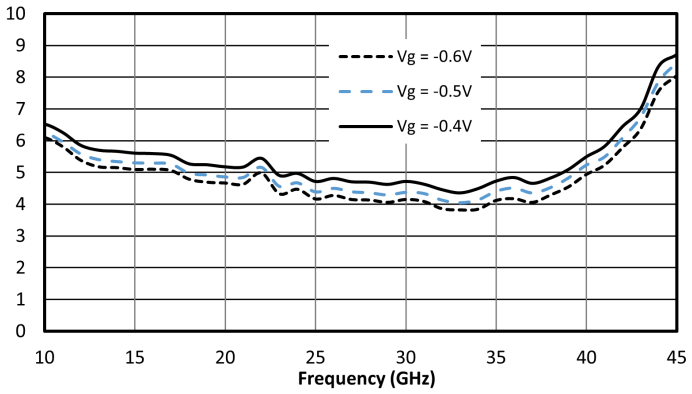
AMM-7199ASM

11-38 GHz GaAs Surface Mount LO Driver Amplifier

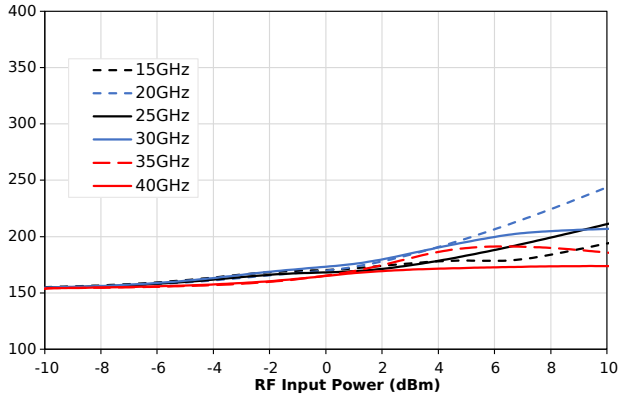
IIP3 (dBm vs Frequency. Vd = +3V



Noise Figure (dB) vs Frequency, Vd = +3V



Drain Current (mA) vs. Input Power and Freq, 3Vd/

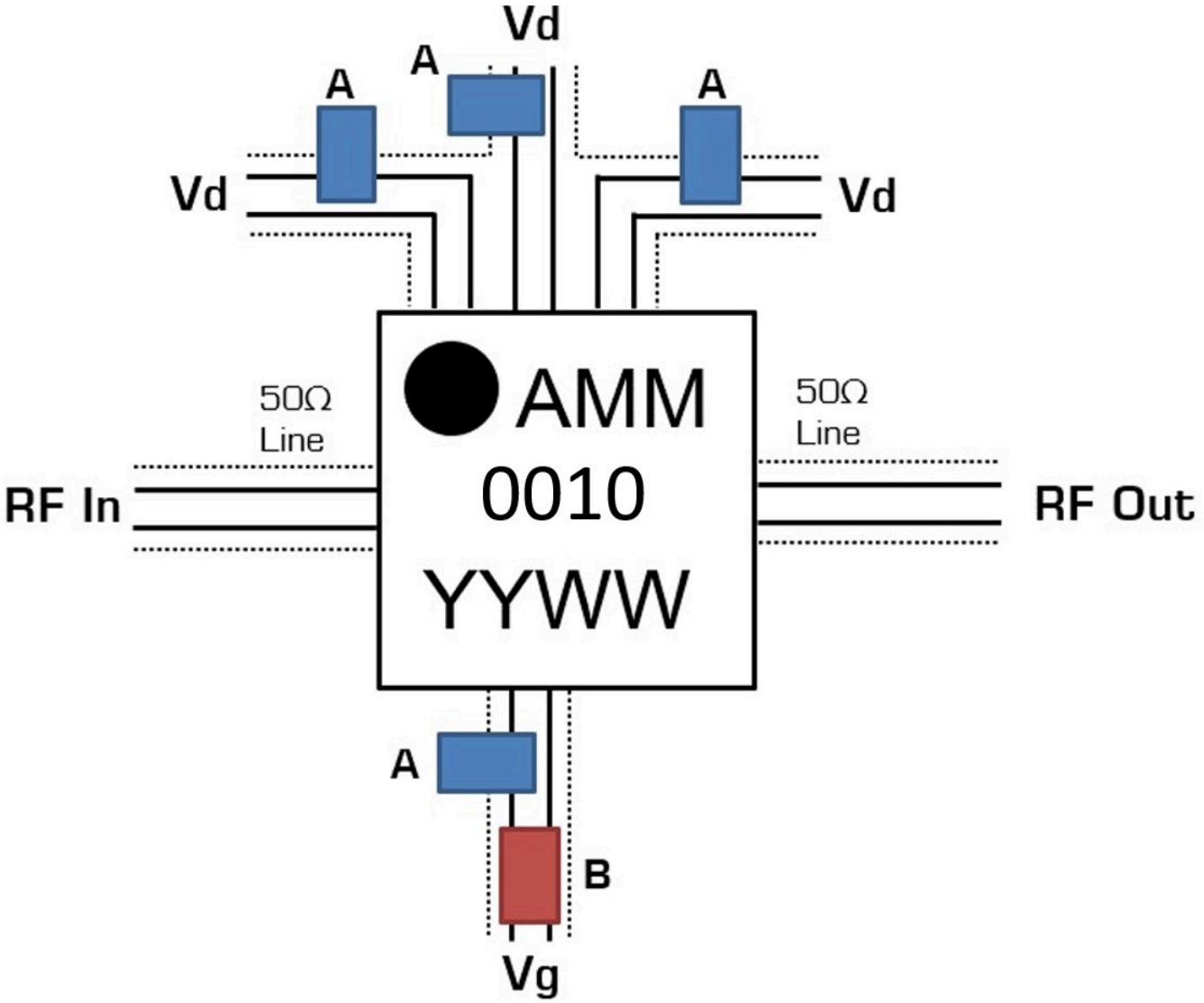


Application Information

Example Application Circuit

Below is the recommended application circuit for the AMM-7199ASM. This is the configuration that is used to characterize this device. However, each PCB layout and environment are different which may require minor modifications of the biasing network.

Application Circuit



Designator	Description	Sample Part Number
A	0.1µF 16V 0402 Capacitor	AVX 0402YD104KAT2A
B	10Ω 0402 Resistor	TE CPF0402B10RE1

Application Circuit Description

The three Vd lines are separated to minimize feedback between the transistor's stages. The passive devices should be 0402 or 0201 surface mount. Examples of suitable passive devices would be the AVX 0402YD104KAT2A capacitor and TE CPF0402B10RE1 resistor. In addition to the resistor and capacitor on the gate pin, the layout of the board should be designed to minimize stray coupling between the drain and gate biasing traces on the board. Additionally, the gate biasing pin AMM-7199ASM can draw up to 0.5mA at certain combinations of frequency and input power.

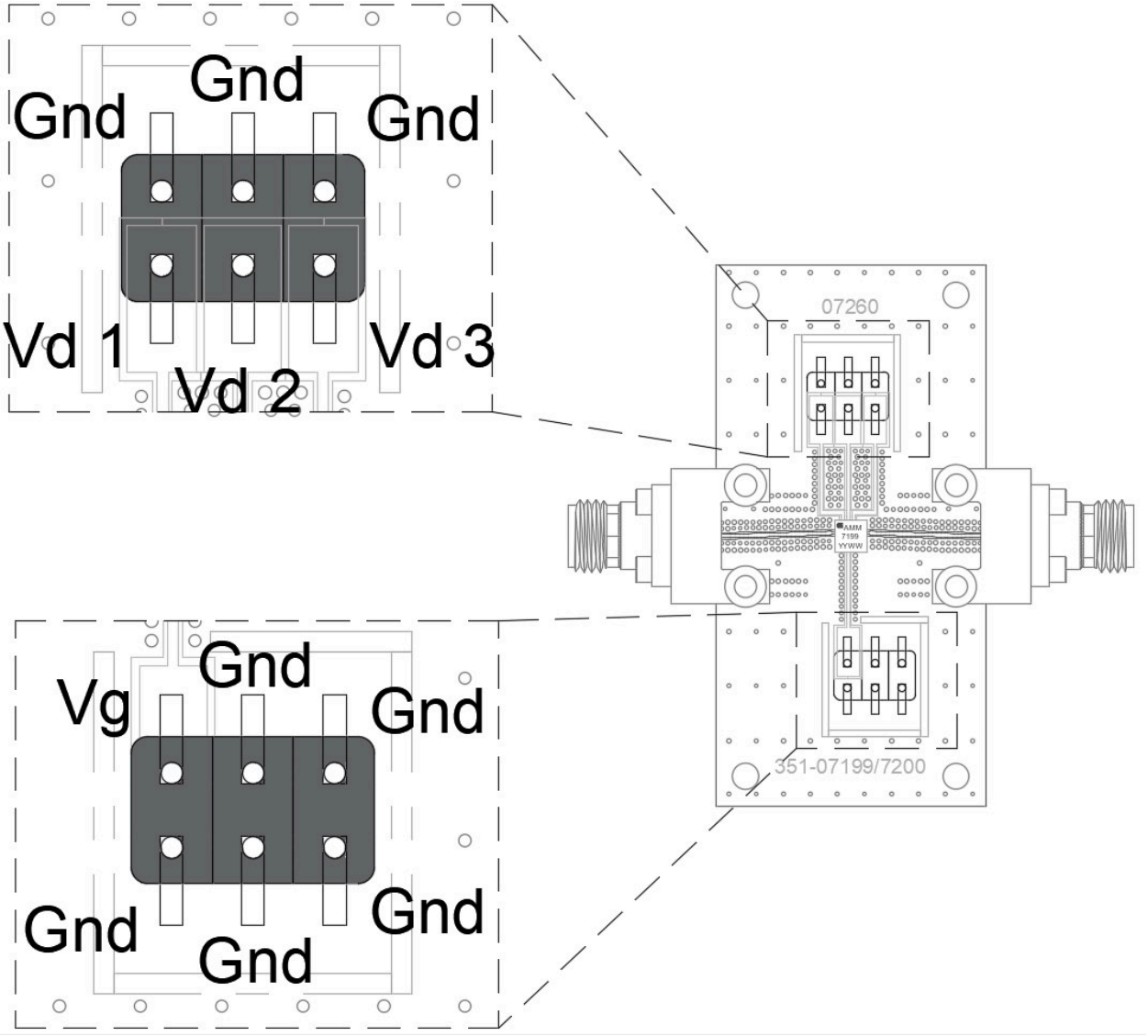
Constant Current and Constant Voltage Operation

The AMM-7199ASM can be biased with a constant gate and drain voltage, or with a constant drain current by regulating the gate voltage. Using a constant gate and drain voltage reduces circuit complexity but has variable current consumption during operation. However, regulating the gate voltage using feedback circuitry which controls the drain current to a constant value minimizes unit-to-unit variation in gain, output power, and compression points.

Under small signal excitation at a fixed temperature, these two approaches are equivalent because the current draw versus frequency is relatively constant in small signal. However, they will diverge in large signal conditions, where the drain current is affected the input signal's frequency and power. The output power in saturation is relatively unchanged, as it is more strongly dependent on the drain voltage. However, output referred 1dB compression point will decrease by 2-3dB when operated with a constant drain current.

Header Pinouts

On the EVB-AMM-7199ASM, there are two headers for biasing the drains and gates of the transistors. The pinout of the headers is given with their location on the evaluation board below:



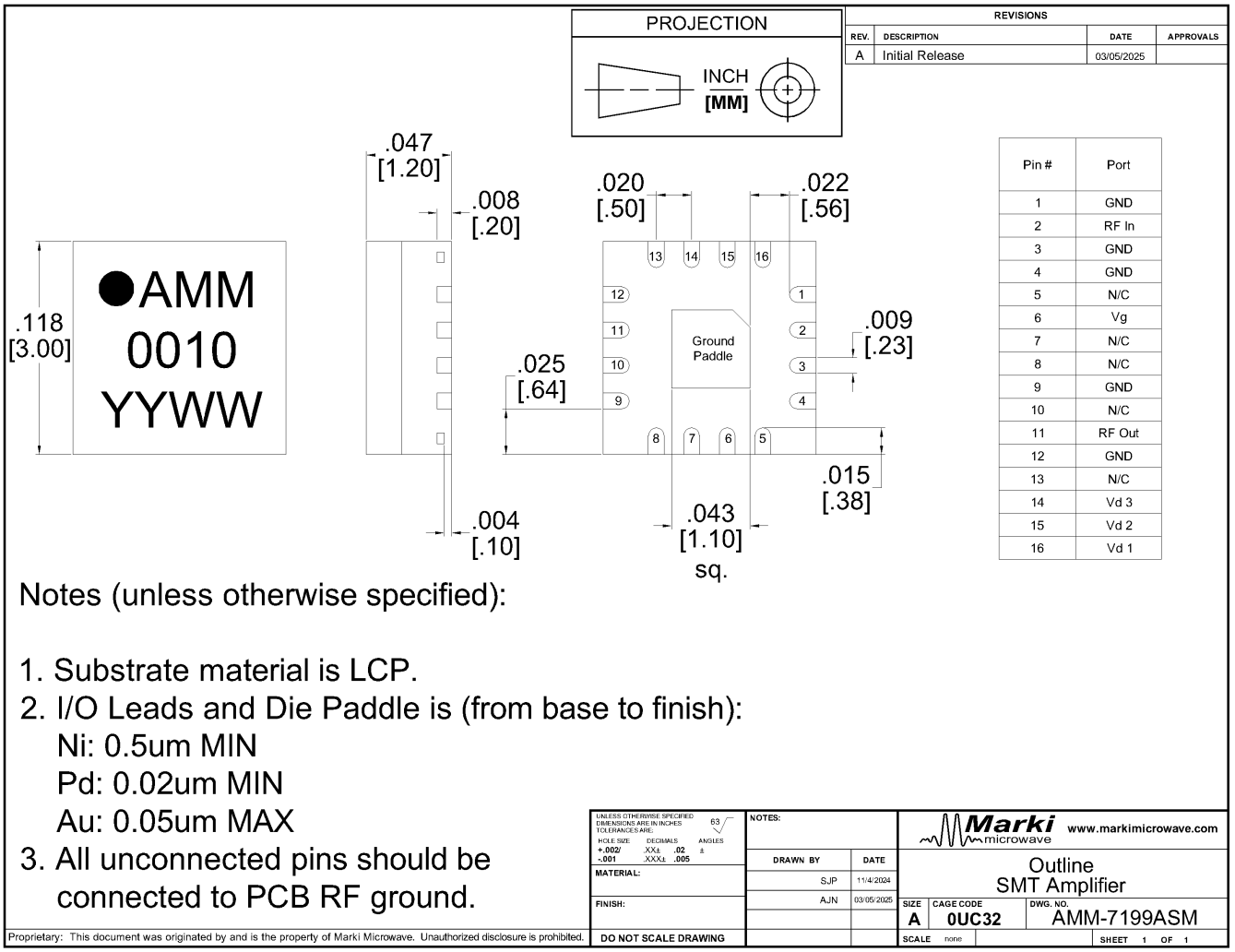
AMM-7199ASM

11-38 GHz GaAs Surface Mount LO Driver Amplifier

Mechanical Data

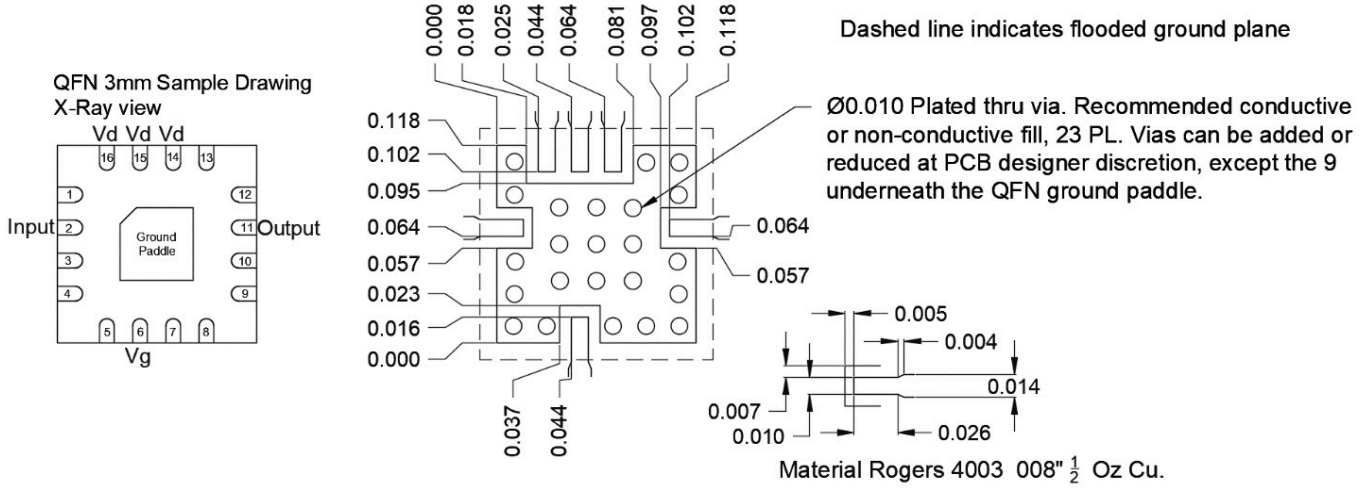
Outline Drawing

Download : Outline 2D Drawing | Outline 3D Drawing | Outline 3D STP

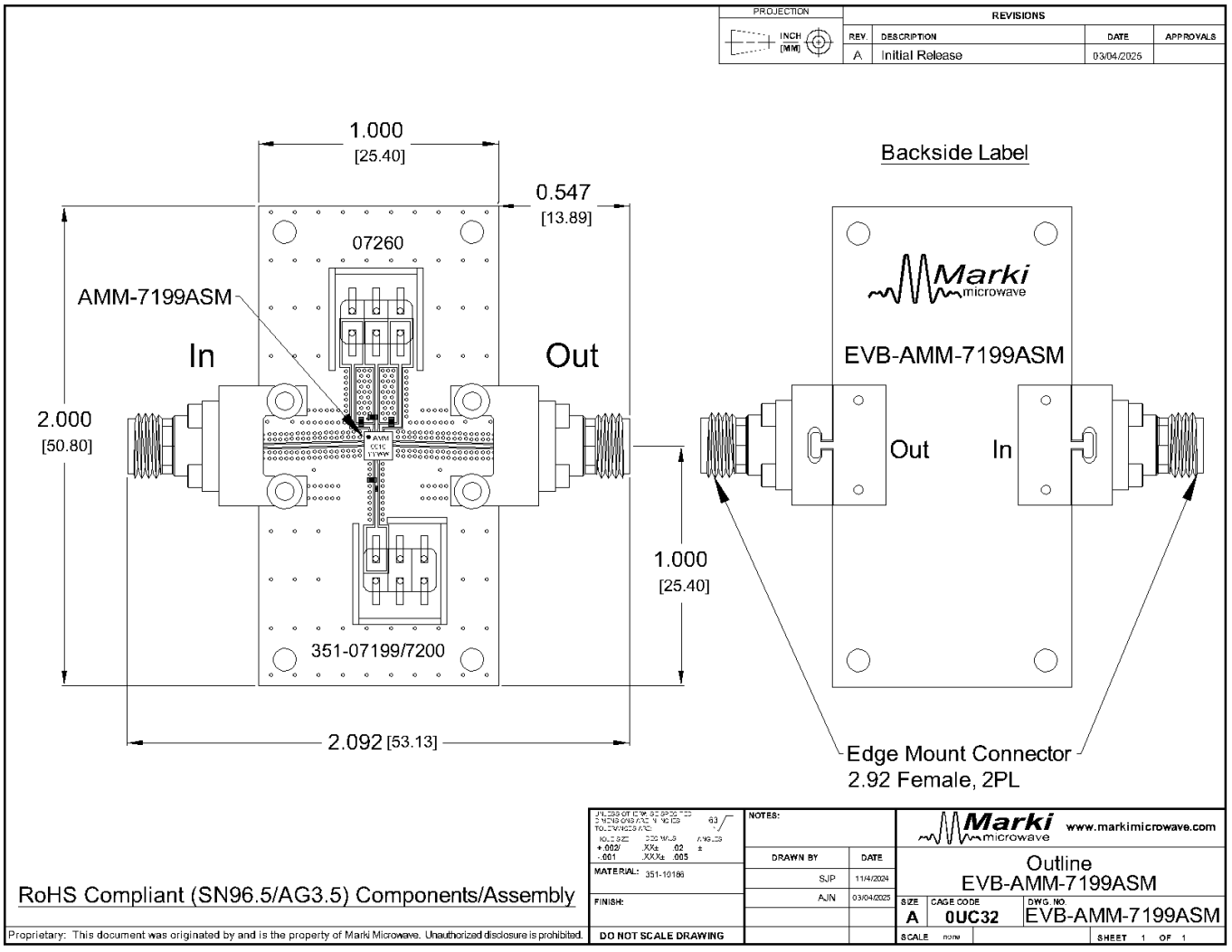


Footprint Image

Download : Footprint Drawing



Evaluation Board - Outline Drawing



DISCLAIMER

MARKI MICROWAVE, LLC., (“MARKI”) PROVIDES TECHNICAL SPECIFICATIONS AND DATA (INCLUDING DATASHEETS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, AND OTHER INFORMATION AND RESOURCES “AS IS” AND WITH ALL FAULTS. MARKI DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT.

These resources are intended for developers skilled in the art designing with Marki products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards and other requirements. Marki makes no guarantee regarding the suitability of its products for any particular purpose, nor does Marki assume any liability whatsoever arising out of your use or application of any Marki product.

Marki grants you permission to use these resources only for development of an application that uses Marki products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Marki intellectual property or to any third-party intellectual property. Marki reserves the right to make changes to the product(s) or information contained herein without notice.