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AMM-7210ACH

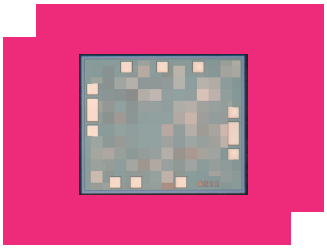
22 - 57 GHz GaAs Driver Amplifier

DEVICE OVERVIEW

General Description

The AMM-7210ACH is a general-purpose broadband MMIC driver amplifier that provides +20 dBm output power suitable for driving a Marki H or L diode mixers at 22-57 GHz and S diode mixers from 25-45 GHz.

Download s-parameters here



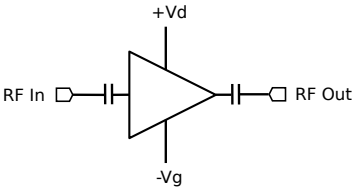
Features

- +20 dBm Output Power
- Broadband Performance
- High Linearity
- Outstanding return loss

Applications

- Mobile test and measurement equipment
- Radar and satellite communications
- 5G transceivers
- Driver amplifier L,H,S – diode mixers

Functional Block Diagram



Part Ordering Options

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
AMM-7210ACH	22 - 57 GHz GaAs Driver Amplifier	CH	REACH RoHS	Released	3A001.b.2.d

Table Of Contents

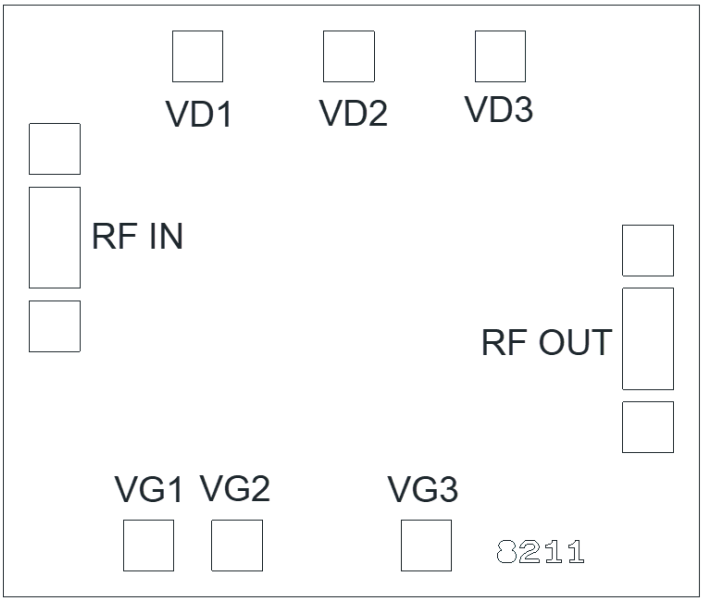
Revision History

Revision Code	Revision Date	Comment
-	2024-09-10	Initial Release
A	2026-02-13	MTTF Table Added.

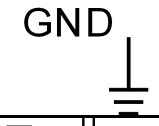
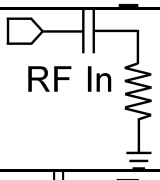
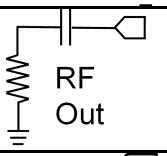
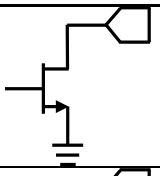
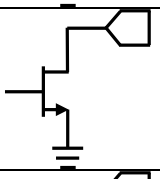
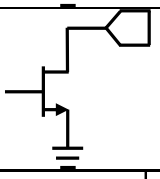
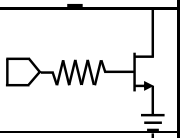
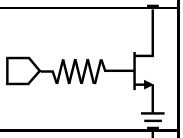
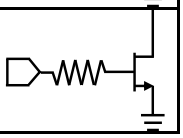
Port Configuration and Functions

Port Diagram

A port diagram of the AMM-7210ACH is shown below.



Port Functions

Port	Function	Description	DC Equivalent Circuit
GND	Ground	Ground is provided through the backside of the die. The backside of the die must be connected to a DC/RF ground with high thermal and electrical conductivity.	
RF In	RF Input	This is the RF Input port of the amplifier die. It is internally DC blocked and RF matched to 50 Ω. RF input pad is GSG with 175um pitch.	
RF Out	RF Output	This is the RF Output port of the amplifier die. It is internally DC blocked and RF matched to 50 Ω. RF output pad is GSG with 175um pitch.	
VD1	Drain Supply Port 1	Pad VD1 supplies the drain voltage to the first stage of the 3-stage amplifier IC. Apply gate voltage to VG pins before applying drain voltage.	
VD2	Drain Supply Port 2	Pad VD2 supplies the drain voltage to the second stage of the 3-stage amplifier IC. Apply gate voltage to VG pins before applying drain voltage.	
VD3	Drain Supply Port 3	Pad VD3 supplies the drain voltage to the third stage of the 3-stage amplifier IC. Apply gate voltage to VG pins before applying drain voltage.	
VG1	Gate Bias Voltage Pad	VG1 provides gate bias to the first stage of the 3-stage amplifier. The user should apply between -0.4 and -0.6V to VG1 pad before applying any VD drain supply.	
VG2	Gate Bias Voltage Pad	VG2 provides gate bias to the second stage of the 3-stage amplifier. The user should apply between -0.4 and -0.6V to VG2 pad before applying any VD drain supply.	
VG3	Gate Bias Voltage Pad	VG3 provides gate bias to the third stage of the 3-stage amplifier. The user should apply between -0.4 and -0.6V to VG3 pad before applying any VD drain supply.	

Specifications

Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If any one of these limits are exceeded, the device may become inoperable or have a reduced lifetime. Reliability limits are individual, instantaneous catastrophic limits only. Functional operation limits are indicated below. Operation of the device at multiple absolute maximum limits or for extended periods at a single limit can cause degradation and damage to the device.

Parameter	Maximum Rating	Unit
Maximum Operating Temperature	85	°C
Maximum Storage Temperature	150	°C
Max Junction Temperature for MTTF of > 1E6 hours	175	°C
Max Power Dissipation for MTTF of > 1E6 hours	1	W
Minimum Operating Temperature	-40	°C
Minimum Storage Temperature	-65	°C
Negative Bias Voltage (Vg)	-2	V
Positive Bias Current	450	mA
Positive Drain Supply Voltage	4.5	V
RF Input Power	20	dBm
θJC, Junction to Case Thermal Resistance	90	°C/W

FIT and MTTF Table

T (°C)	λ (TIF)	MTTF (hr)	MTTF (yr)
105	2,441.45	4.10E+05	47
85	310.48	3.22E+06	368
55	8.79	1.14E+08	12,992
25	0.12	8.24E+09	941,063

Package Information

Parameter	Details	Rating
Dimensions	-	1.38 x 1.17 mm

Recommended Operating Conditions

The Recommended Operating Conditions indicate the limits, inside which the device should be operated, to guarantee the performance given in Electrical Specifications Operating outside these limits may not necessarily cause damage to the device, but the performance may degrade outside the limits of the electrical specifications. For limits, above which damage may occur, see Absolute Maximum Ratings.

Parameter	Min	Nominal	Max	Unit
Gate Bias DC Voltage (Vg)	-0.6	-0.5	-0.4	V
Positive DC Voltage (Vd)	2.5	3	3	V
Ambient Temperature	-55	25	85	°C
Positive DC Current (Id) (No RF Input)	100	150	200	mA

Sequencing Requirements

Turn-on Procedure:
1. Apply negative bias to Vg
2. Apply Vd

Turn-off Procedure:
1. Turn off Vd
2. Turn off Vg

Note: RF input power can be injected at any moment in the bias sequencing procedure.

Electrical Specifications

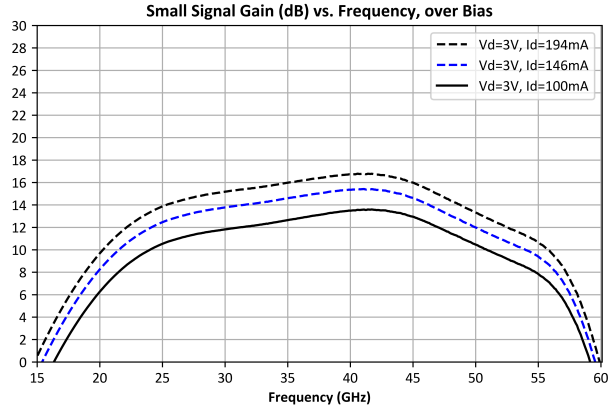
The electrical specifications apply at TA=+25°C in a 50Ω system. Min and Max limits apply only to our connectorized units and are guaranteed at TA=+25°C. Die are 100% DC tested and RF tested on a per lot basis

Parameter	Test Conditions	Minimum Frequency (GHz)	Maximum Frequency (GHz)	Min	Typ	Max	Unit
Current Consumption [1]	+3V, Vg=-0.5V	-	-	-	150	-	mA
Input IP3	+3V, Id=150mA, -20dBm Input Power	22	40	-	15	-	dBm
Input IP3	+3V, Id=150mA, -20dBm Input Power	40	57	-	12	-	dBm
Input Power for Saturation	+3V, Id=150mA	22	57	-	8	-	dBm
Input Return Loss	+3V, Id=150mA	22	57	-	14	-	dB
Noise Figure	+3V, Id=150mA	22	57	-	5.8	-	dB
Output IP3	+3V, Id=150mA, -20dBm Input Power	40	57	-	25	-	dBm
Output IP3	+3V, Id=150mA, -20dBm Input Power	22	40	-	28	-	dBm
Output P1dB	+3V, Id=150mA	27	57	-	18.5	-	dBm
Output P1dB	+3V, Id=150mA	22	27	-	17	-	dBm
Output Return Loss	+3V, Id=150mA	22	57	-	12	-	dB
Reverse Isolation	+3V, Id=150mA	22	57	-	55	-	dB
Saturated Output Power	+3V, Id=150mA	22	25	-	19	-	dBm
Saturated Output Power	+3V, Id=150mA	25	45	-	20	-	dBm
Saturated Output Power	+3V, Id=150mA	45	57	-	17	-	dBm
Small Signal Gain	+3V, Id=150mA	50	57	-	10	-	dB
Small Signal Gain	+3V, Id=150mA	25	50	10	14.5	-	dB
Small Signal Gain	+3V, Id=150mA	22	25	-	11.5	-	dB

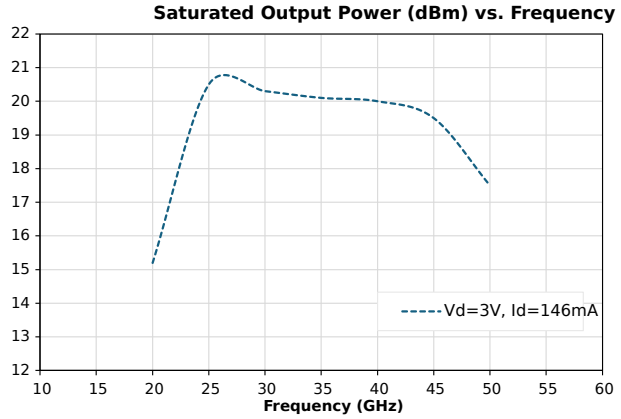
[1] Bias conditions tested with no RF input power.

Typical Performance Plots

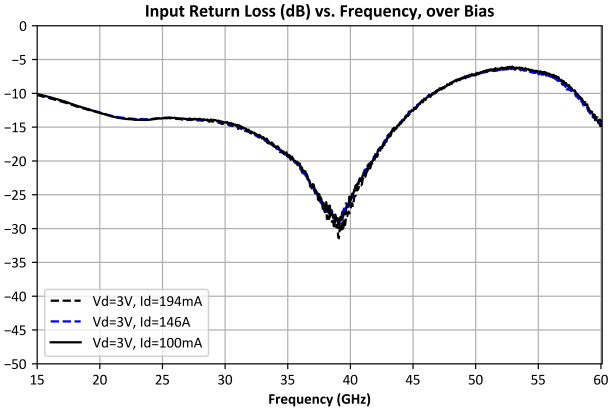
Small Signal Gain (dB) vs. Frequency, over Bias



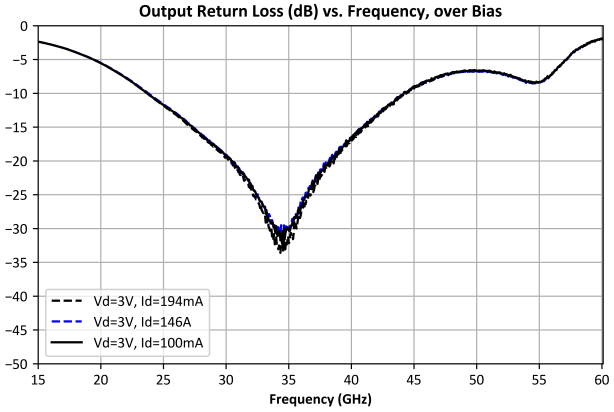
Saturated Output Power (dBm) vs. Frequency



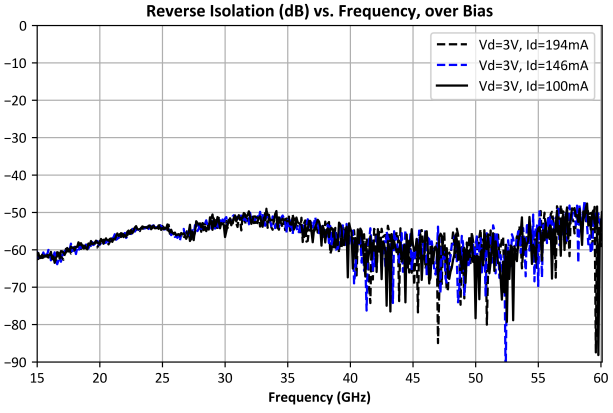
Input Return Loss (dB) vs. Frequency, over Bias



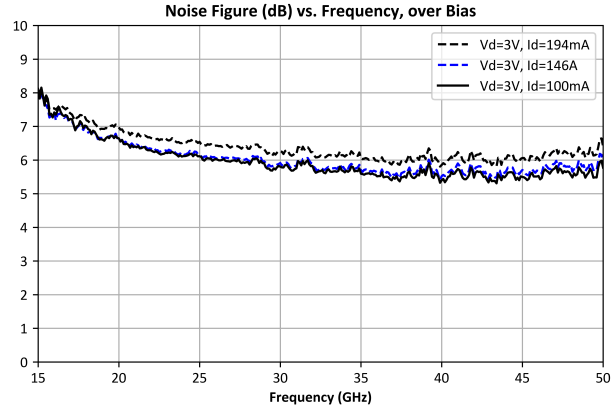
Output Return Loss (dB) vs. Frequency, over Bias



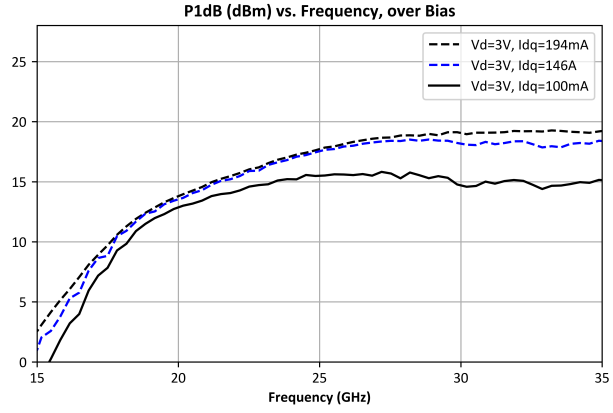
Reverse Isolation (dB) vs. Frequency, over Bias



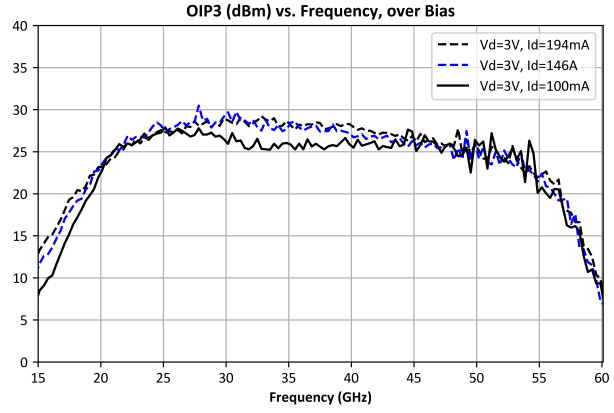
Noise Figure (dB) vs. Frequency, over Bias

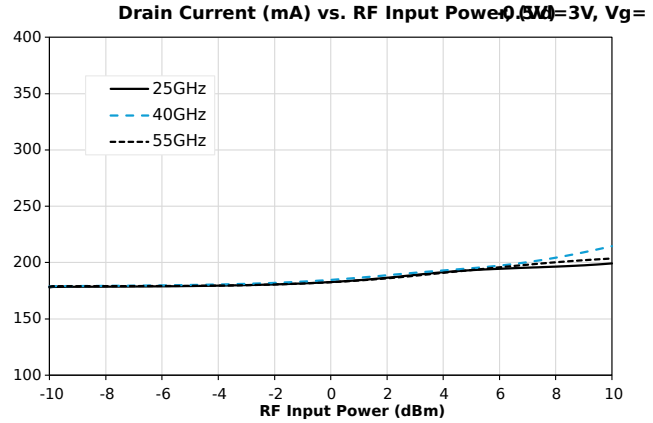


P1dB (dBm) vs. Frequency, over Bias



OIP3 (dBm) vs. Frequency, over Bias

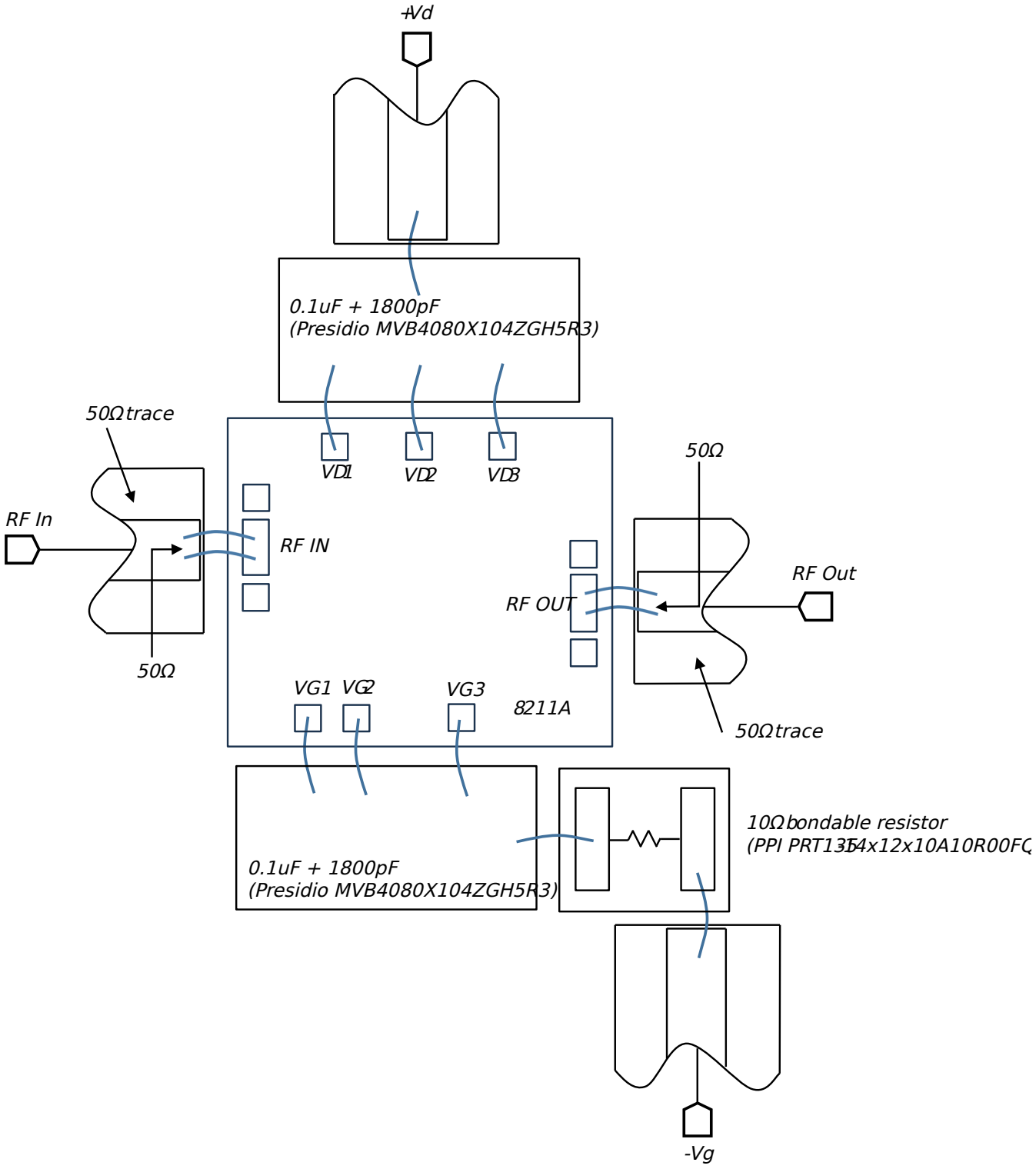




Application Information

The application circuit for the AMM-7210ACH is shown below.

Application Circuit



Application Circuit Description

Constant Drain Current vs. Constant Gate Voltage Operation

The AMM-7210A pHEMT amplifier can be biased with a constant gate and drain voltage, or with a constant drain current by regulating the gate voltage. Using a constant gate and drain voltage reduces circuit complexity, but has variable current consumption during operation. However, regulating the gate voltage using feedback circuitry which controls the drain current to a constant value minimizes unit-to-unit variation in gain, output power, and compression points.

Under small signal excitation at a fixed temperature, these two approaches are equivalent because the current draw versus frequency is relatively constant in small signal. However, they will diverge in large signal conditions, where the drain current is affected the input signal's frequency and power. The output power in saturation is relatively unchanged, as it is more strongly dependent on the drain voltage. However, output referred 1 dB compression point will decrease by 2-3 dB when operated with a constant drain current.

Die Mounting Recommendations

Mounting and Bonding Recommendations

Marki MMICs should be attached directly to a ground plane with conductive epoxy. The ground plane electrical impedance should be as low as practically possible. This will prevent resonances and permit the best possible electrical performance. Datasheet performance is only guaranteed in an environment with a low electrical impedance ground.

Mounting - To epoxy the chip, apply a minimum amount of conductive epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip.Cure epoxy according to manufacturer instructions.

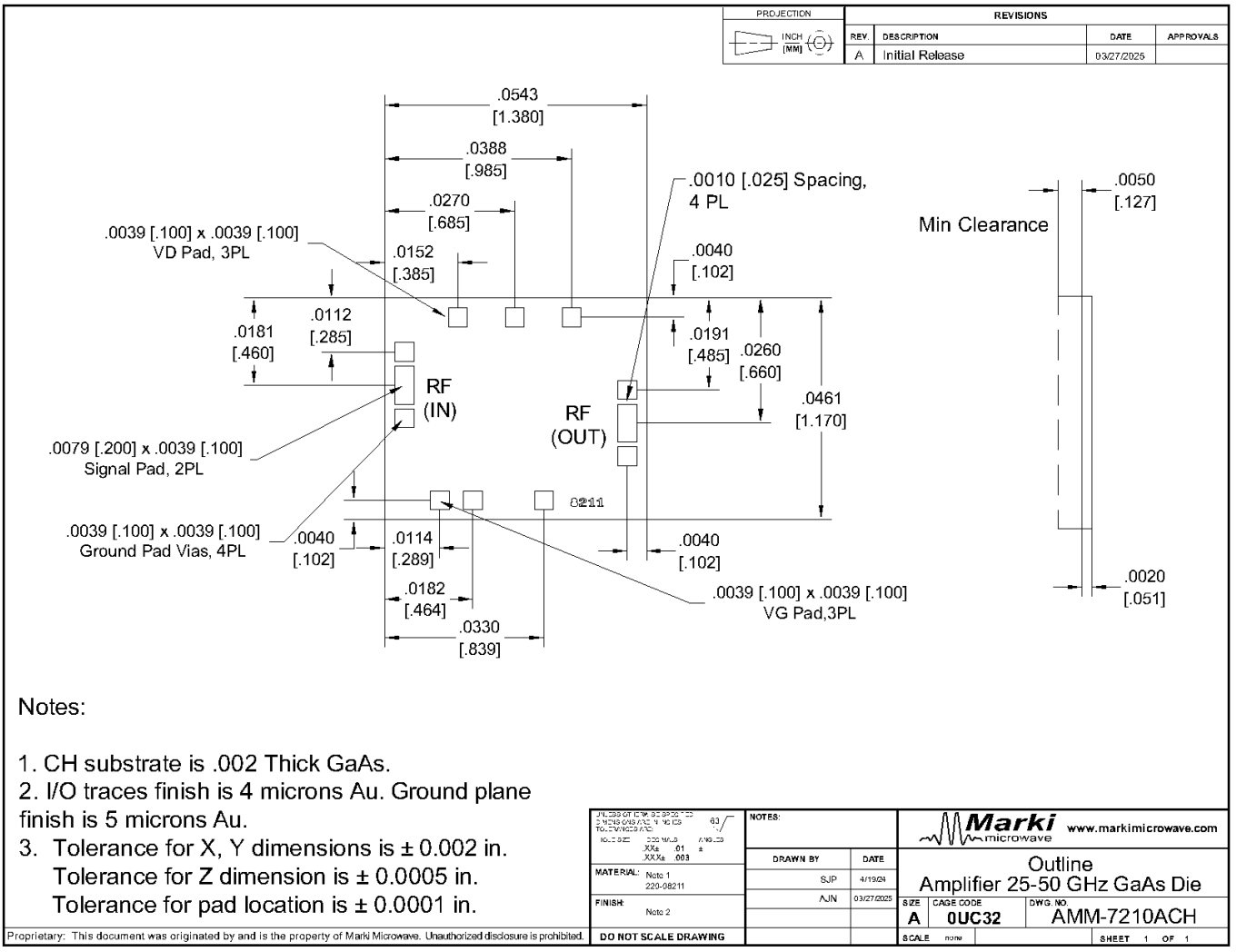
Wire Bonding - Ball or wedge bond with 0.025 mm (1 mil) diameter pure gold wire.Thermosonic wirebonding with a nominal stage temperature of 150 °C and a ball bonding force of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Use the minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should be started on the chip and terminated on the package or substrate. Bond wire inductance will improve return loss. Bondwire inductance in the range of 30pH to 200pH will improve performance.

Circuit Considerations – 50 Ω transmission lines should be used for all high frequency connections in and out of the chip. Wirebonds should be kept as short as possible, with multiple wirebonds recommended for higher frequency connections to reduce parasitic inductance. In circumstances where the chip more than .001” thinner than the substrate, a heat spreading spacer tab is optional to further reduce bondwire length and parasitic inductance.

Mechanical Data

Outline Drawing

Download : Outline 2D Drawing



Notes:

1. CH substrate is .002 Thick GaAs.
2. I/O traces finish is 4 microns Au. Ground plane finish is 5 microns Au.
3. Tolerance for X, Y dimensions is ± 0.002 in.
Tolerance for Z dimension is ± 0.0005 in.
Tolerance for pad location is ± 0.0001 in.

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