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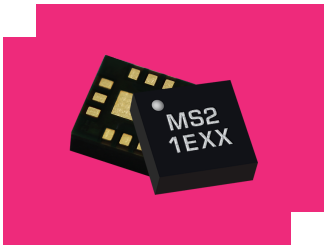
MSW2-1001ELGA

0.1-40 GHz Surface Mount SPDT Switch

DEVICE OVERVIEW

General Description

The MSW2-1001ELGA is a reflective, single-pole double throw (SPDT) switch. The part is manufactured using a Silicon-On-Insulator (SOI) process. The switch operates from 100MHz to 40GHz with average insertion loss and isolation of 1.2dB and 40dB respectively and input power handling and hot switching capability of 27 dBm. The MSW2-1001ELGA requires positive and negative 3.3V supply inputs and is controlled via a single input pin compatible with LVTTL logic. This switch has a 50-Ohm characteristic impedance. The MSW2-1001ELGA is packaged in a compact 2.25x2.25 mm LGA for surface mount integration on circuit board-based systems.



Download s-parameters here

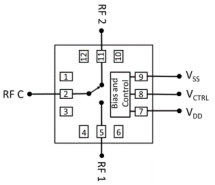
Features

- Wide Bandwidth (0.1 - 40GHz)
- Low Insertion loss
- High Isolation
- Hot Switching Capable
- Internal Supply Regulation
- Low Power Consumption

Applications

- Mobile test and measurement equipment
- Radar
- SATCOM
- Electronic Warfare
- 5G

Functional Block Diagram



Part Ordering Options

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
MSW2-1001ELGA	0.1-40 GHz Surface Mount SPDT Switch	LGA	REACH RoHS	Released	EAR99
EVB-MSW2-1001E	0.1 - 40 GHz Surface Mount SPDT Switch	EVB	REACH RoHS	Released	EAR99

Table Of Contents

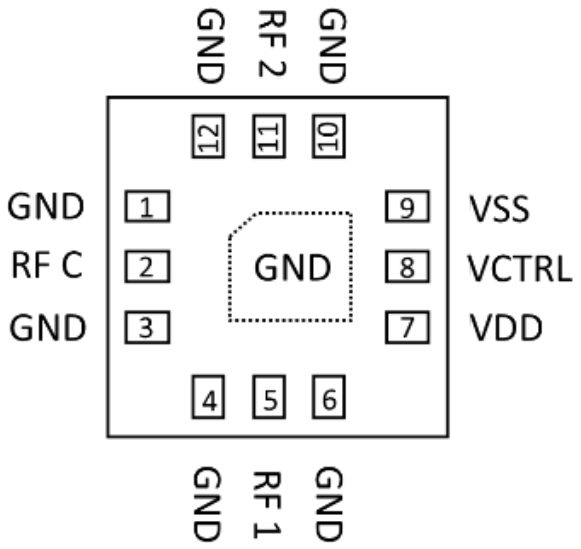
Revision History

Revision Code	Revision Date	Comment
-	2022-06-01	Initial Datasheet Release
A	2025-05-13	Vctrl Logic Table Updated

Port Configuration and Functions

Port Diagram

A port diagram of the MSW2-1001ELGA is shown below. (View looking down from the top side.)



Port Functions

Port	Function	Description	DC Equivalent Circuit
11	RF2	RF port 2 of the device, impedance looking into this port matches RFC load impedance in the ON state. This port is reflective and shorted to GND in the OFF state. This port is DC coupled. A DC blocking capacitor is required ONLY if max DC voltages will be exceeded.	-
1,3,4,6,10,12	Ground	These pins should be connected to RF/DC ground. All GND pins are internally connected.	-
2	RFC	RF common port of the device. This port is DC coupled. A DC blocking capacitor is required ONLY if max DC voltages will be exceeded. This port has a 50 Ohm input impedance when the active port is terminated with a 50 Ohm load.	-
5	RF1	RF port 1 of the device, impedance looking into this port matches RFC load impedance in the ON state. This port is reflective and shorted to GND in the OFF state. This port is DC coupled. A DC blocking capacitor is required ONLY if max DC voltages will be exceeded.	-
7	VDD	Positive DC supply pin. (+3.3V). Port has an ESD clamp to GND.	-
8	VCTRL	Control voltage input pin. Low Voltage Transistor-Transistor Logic (LVTTL) compatible. Port has ESD clamp to GND and VDD. An external pull-down resistor is recommended on this pin.	-
9	VSS	Negative DC supply pin. (-3.3V). Port has an ESD clamp to GND.	-
Paddle	Ground	IC backside must be connected to a DC/RF ground with high thermal and electrical conductivity.	-

Specifications

Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If these limits are exceeded, the device may become inoperable or have a reduced lifetime.

Parameter	Maximum Rating	Unit
Control Voltage	3.9	V
Max Current on any RF Port, Unbiased	50	µA
Max DC on any RF Port, Unbiased	0.5	V
Max Hot Switching RF Input Power	27	dBm
Maximum Operating Temperature for MTTF > 1E6 hours	105	°C
Maximum Storage Temperature	150	°C
Max Junction Temperature for MTTF of > 1E6 hours	135	°C
Max Power Dissipation for MTTF of > 1E6 hours at 85°C Baseplate Temperature	140	mW
Negative Supply Voltage	-3.6	V
Positive Supply Voltage	3.6	V
RF Input Power, Nominal Bias	27.5	dBm
RF Input Power, Unbiased	21	dBm
θJC, Junction to Ambient Thermal Resistance	352	°C/W

Package Information

Parameter	Details	Rating
ESD	250 to < 500 Volts	HBM Class 1A
Dimensions	-	2.25 x 2.25 mm
Moisture Sensitivity Level	-	MSL 3

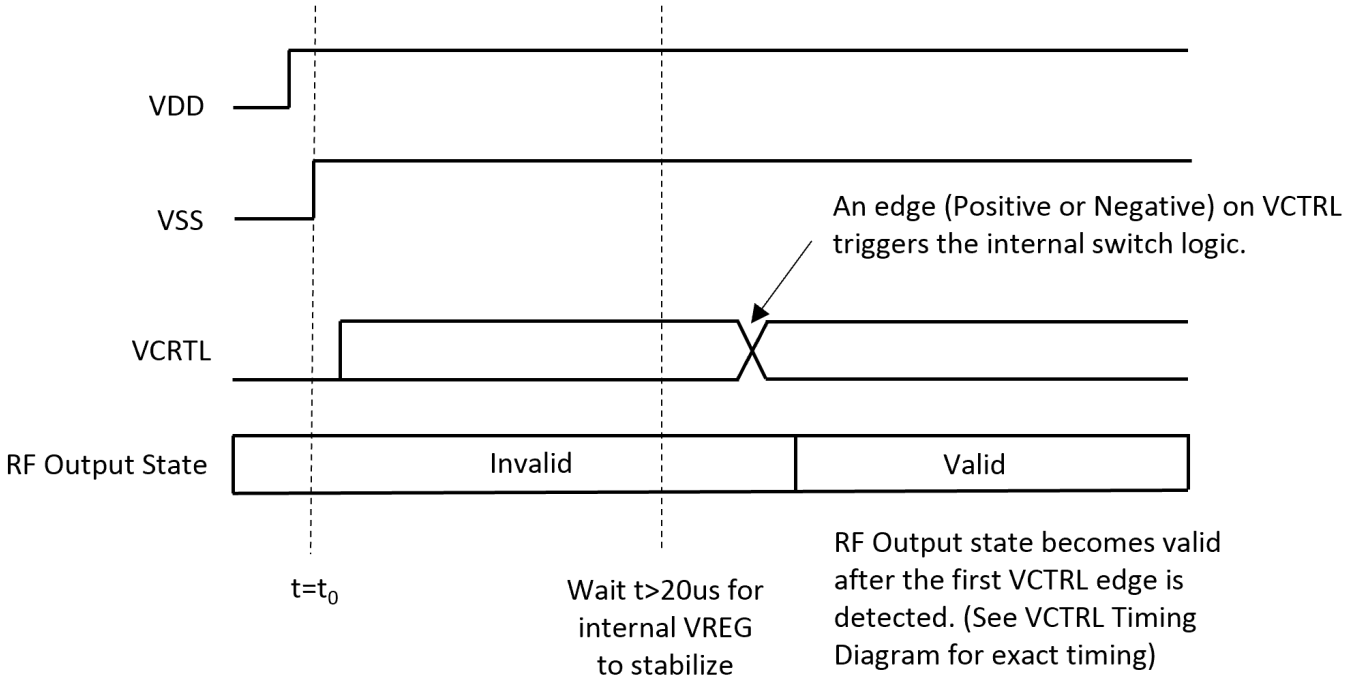
Recommended Operating Conditions

The Recommended Operating Conditions indicate the limits, inside which the device should be operated, to guarantee the performance given in Electrical Specifications. Operating outside these limits may not necessarily cause damage to the device, but the performance may degrade outside the limits of the electrical specifications. For limits, above which damage may occur, see Absolute Maximum Ratings.

Parameter	Min	Nominal	Max	Unit
Ta Ambient Temperature	-40	25	101	°C
Positive DC Voltage	3.15	3.3	3.45	V
Negative DC Voltage	-3.45	-3.3	-3.15	V
Positive Supply Current	-	590	-	µA
Negative Supply Current	-	660	-	µA
Control Voltage Low, VINL	0	-	1.55	V
Control Current, IINL	-	-	1	µA
Control Current, IINH	-	-	1	µA
Control Voltage High, VINH	1.63	-	3.45	V

Sequencing Requirements

The startup sequence for the switch should be as follows (required only on initial startup of the device):
1) Apply V_{DD}
2) Apply V_{SS}
3) Wait >20us (Waiting for internal V_{REG} to stabilize and power internal logic)
a. VCTRL may be safely applied during this time but will produce un-predictable output until after 20us when the internal regulator has stabilized.
4) Apply V_{CTRL} (See Diagram Below)

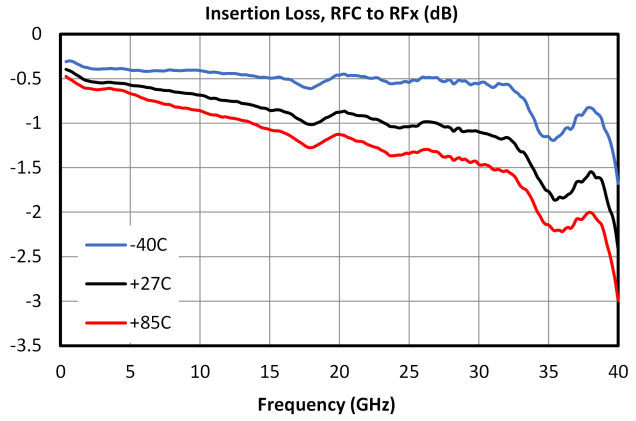


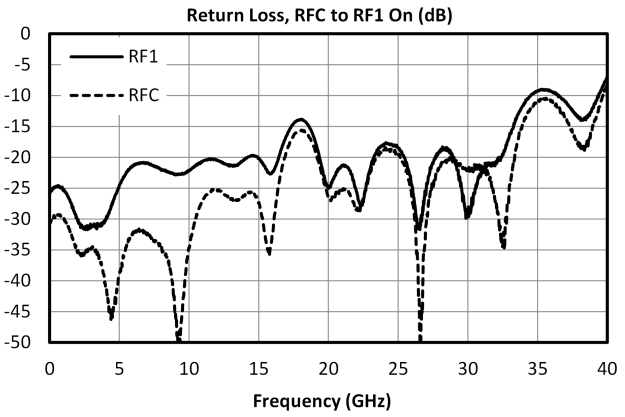
Electrical Specifications

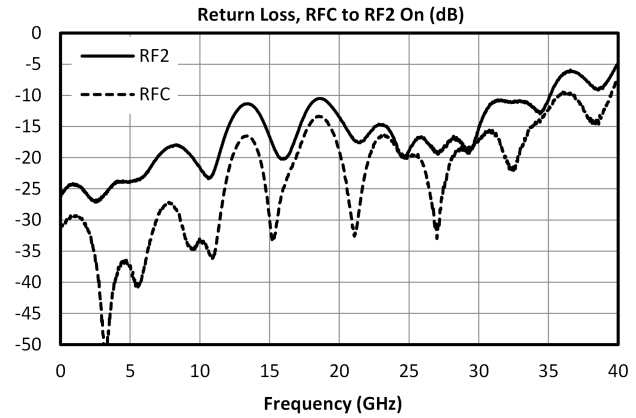
The electrical specifications apply at TA=+25 °C in a 50 Ω system. Unless otherwise noted, all specifications are for VDD=3.3V, VSS=-3.3V and VCTRL = 0 or 3.3V (both switch paths) with all ports terminated into 50 Ω loads.

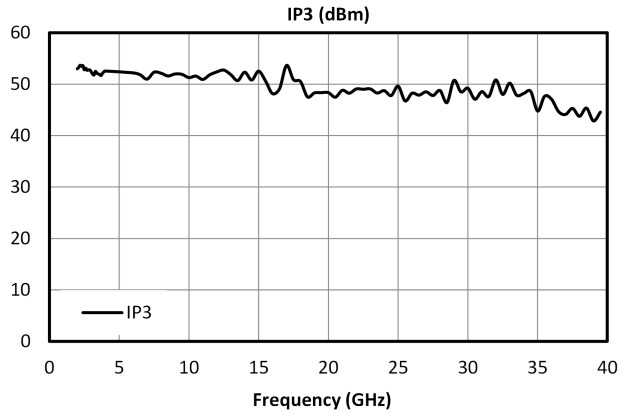
Parameter	Test Conditions	Minimum Frequency (GHz)	Maximum Frequency (GHz)	Min	Typ	Max	Unit
Input 0.1dB Compression Point	Vdd=3.3V, Vss=-3.3V, Vctrl = 0 or 3.3V	2	18	-	27	-	dBm
Input IP3	Two Tones @ +12dBm, dF = 1 MHz	2	40	-	50	-	dBm
Insertion Loss	Vdd=3.3V, Vss=-3.3V, Vctrl = 0 or 3.3V	35	40	-	1.5	-	dB
Insertion Loss	Vdd=3.3V, Vss=-3.3V, Vctrl = 0 or 3.3V	0.1	18	-	0.7	-	dB
Insertion Loss	Vdd=3.3V, Vss=-3.3V, Vctrl = 0 or 3.3V	18	35	-	1	-	dB
Isolation, RF1 to RF2	Vdd=3.3V, Vss=-3.3V, Vctrl = 0 or 3.3V	35	40	-	43	-	dB
Isolation, RF1 to RF2	Vdd=3.3V, Vss=-3.3V, Vctrl = 0 or 3.3V	0.1	18	-	57	-	dB
Isolation, RF1 to RF2	Vdd=3.3V, Vss=-3.3V, Vctrl = 0 or 3.3V	18	35	-	47	-	dB
Isolation, RFC to any non-active Port	Vdd=3.3V, Vss=-3.3V, Vctrl = 0 or 3.3V	35	40	-	38	-	dB
Isolation, RFC to any non-active Port	Vdd=3.3V, Vss=-3.3V, Vctrl = 0 or 3.3V	0.1	18	-	47	-	dB
Isolation, RFC to any non-active Port	Vdd=3.3V, Vss=-3.3V, Vctrl = 0 or 3.3V	18	35	-	40	-	dB
Make-before-break overlap	-	0.1	40	-	36	-	ns
Negative Supply Current	Vdd = 3.3V, Vss = -3.3V, Vctrl = 0 or 3.3V	-	-	-	660	-	µA
Nominal RF Impedance	Vdd = 3.3V. Vss = -3.3V, Vctrl = 0 or 3.3V	-	-	-	50	-	Ω
Off-Time	50% VCTRL to 90% RF output	0.1	40	-	85	-	ns
On-Time	50% VCTRL to 90% RF output	0.1	40	-	85	-	ns
Positive Supply Current	Vdd = 3.3V, Vss = -3.3V, Vctrl = 0 or 3.3V	-	-	-	590	-	µA
Return Loss	Vdd=3.3V, Vss=-3.3V, Vctrl = 0 or 3.3V	35	40	-	11	-	dB
Return Loss	Vdd=3.3V, Vss=-3.3V, Vctrl = 0 or 3.3V	0.1	18	-	24	-	dB
Return Loss	Vdd=3.3V, Vss=-3.3V, Vctrl = 0 or 3.3V	18	35	-	22	-	dB
RF Settling Time	50% VCTRL to 0.05dB final RF output	0.1	40	-	95	-	ns
RF Settling Time	50% VCTRL to 0.1dB final RF output	0.1	40	-	90	-	ns
Risetime/Falltime	10-90% of RF output	0.1	40	-	10	-	ns
VCTRL Latency	50% VCTRL to start of RF state transition	0.1	40	-	45	-	ns

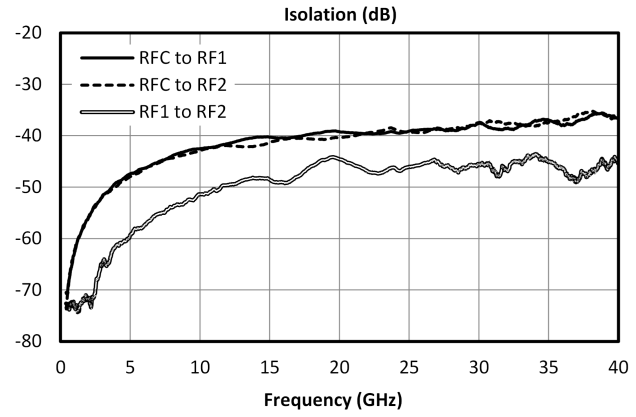
Typical Performance Plots

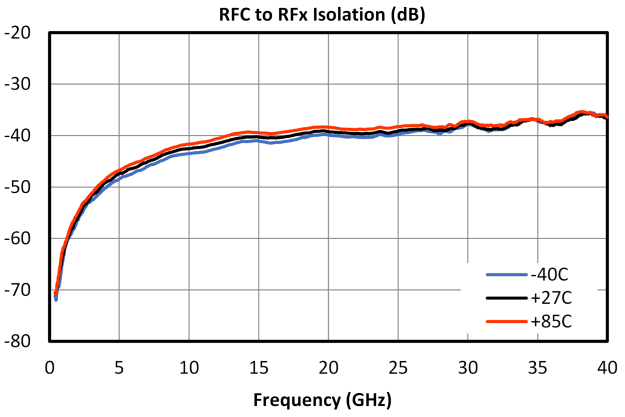


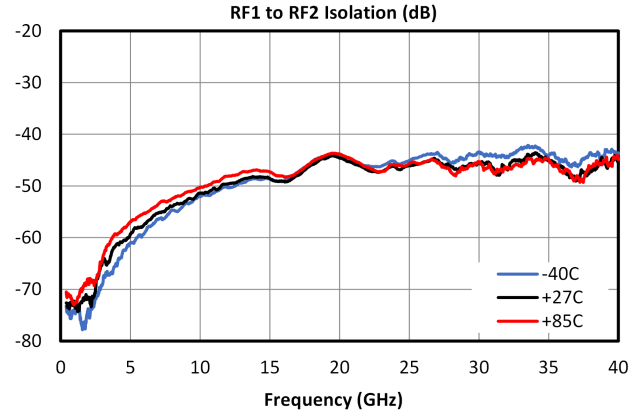


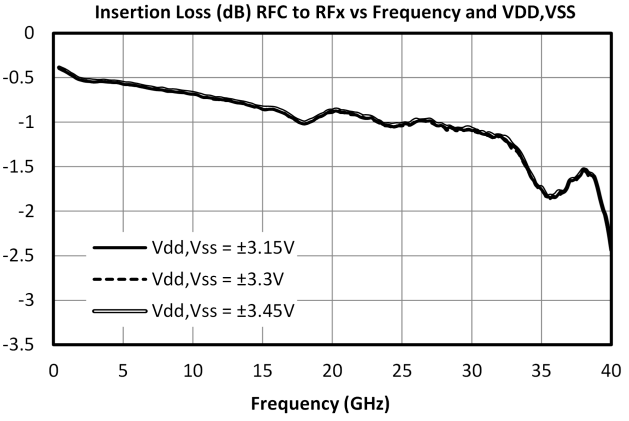






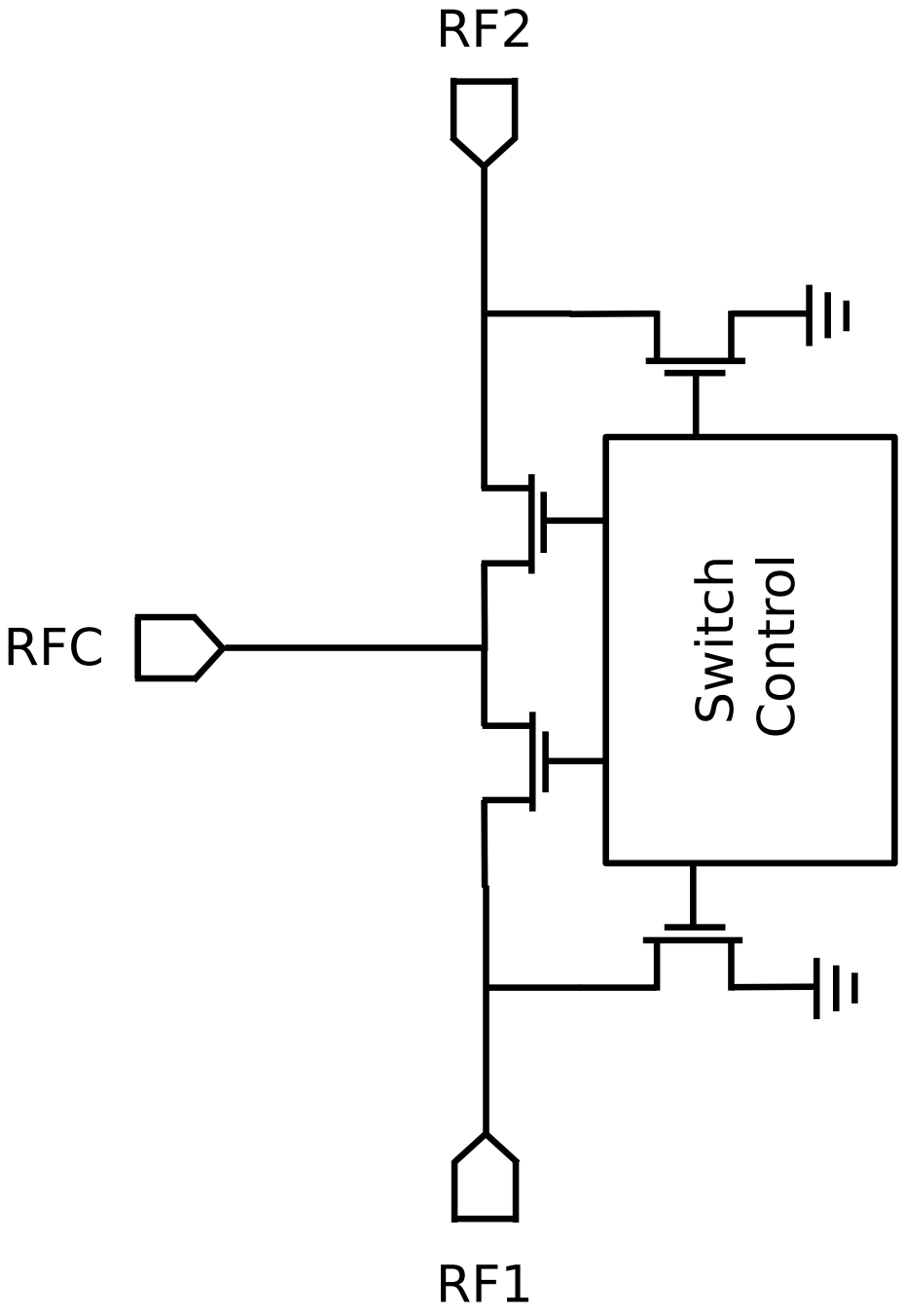






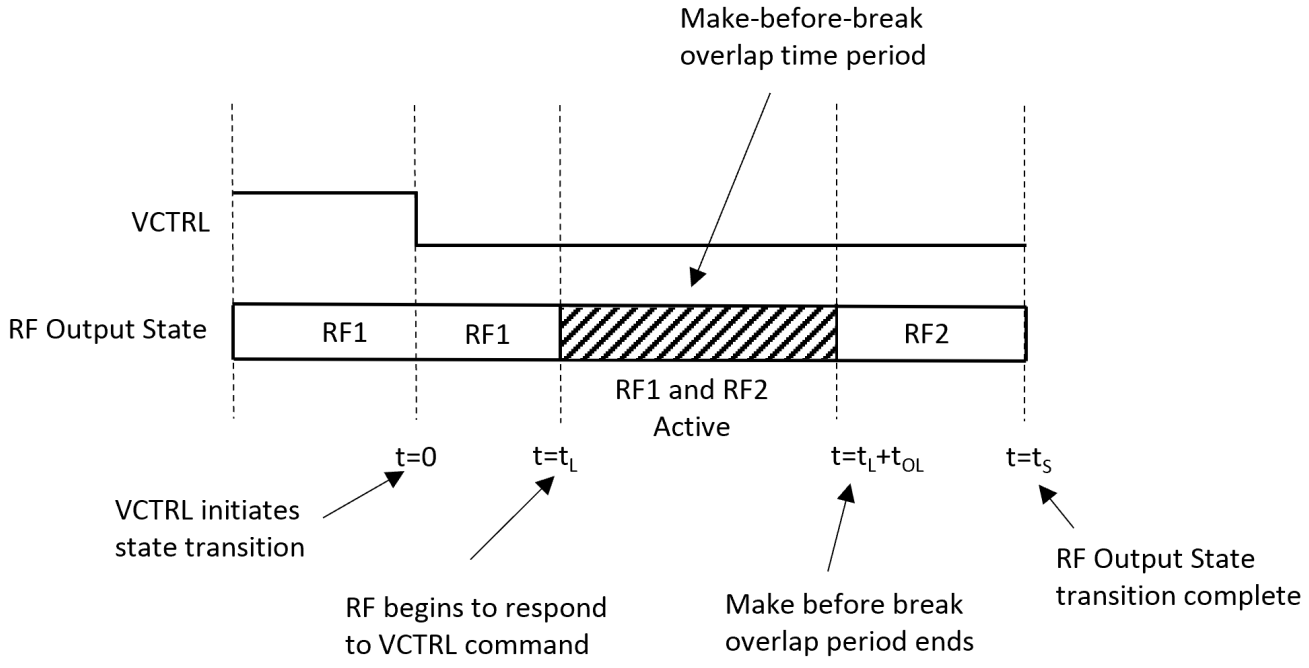
Application Information

The MSW2-1001ELGA is an RF SPDT switch built on an SOI process. The switch is designed with two main-branches, each having a corresponding shunt-branch switch to GND. The shunt-branches exist to improve off-state isolation of each port. When each main-branch switch is activated, the associated shunt-branch is de-activated. Likewise, when the main-branch switches are de-activated, the associated shunt-branch switch is activated. Thus, ports RF1 and RF2 appear internally matched to 50 ohms while in the on-state and are reflective (short to GND) when in the off-state. The RFC port is internally matched to 50 ohms.



RF Switch Configuration

The MSW2-1001ELGA is capable of hot-switching powers up to +27dBm. Hot-switching is enabled by a “make-before-break” circuit in the switch. This circuit acts to safely transition power to the newly active switch branch from the previously active switch branch. There is a period of time when both switch states are active during the state transition. See the timing diagram below for details on the timing of the switch transition between states.



Switch Timing Diagram

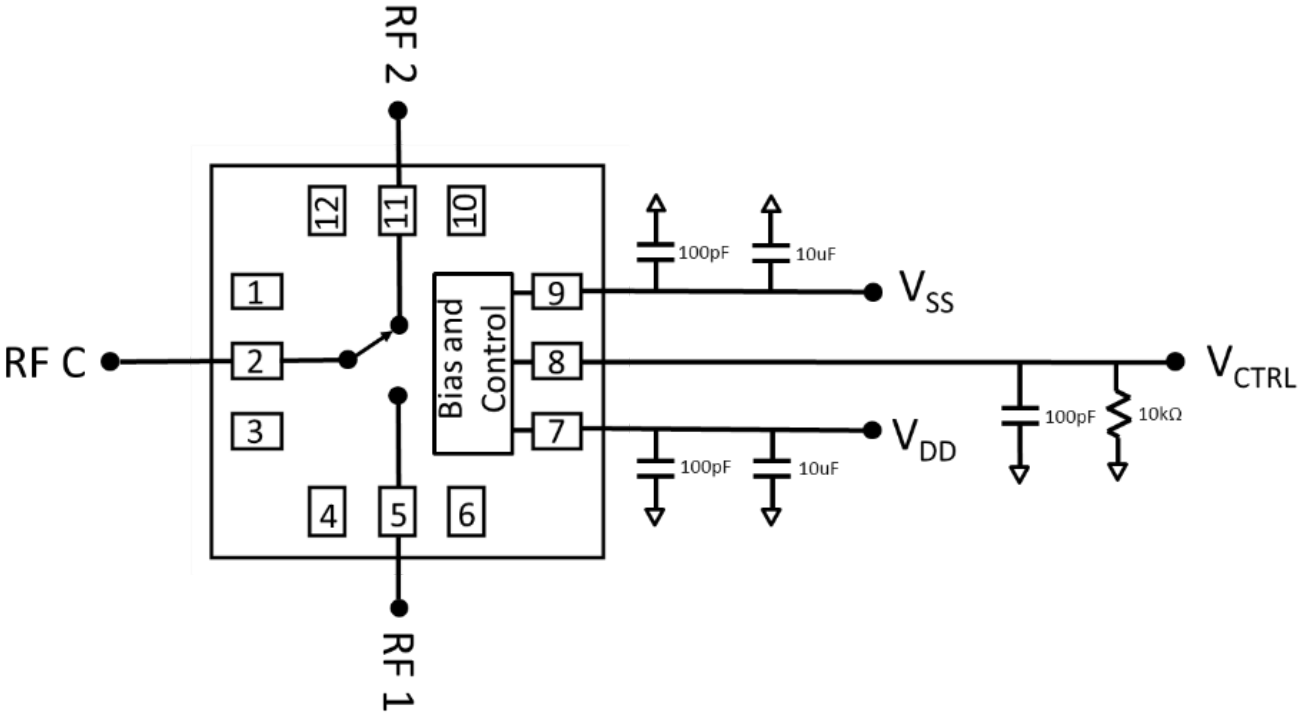
The MSW2-1001ELGA requires both positive and negative 3.3V supply voltages. Supply voltages are internally regulated to minimize the impact of transient supply voltage variations. Bypassing capacitors are recommended on both supply lines. (See 5.2 Application Schematic)

The V_{CTRL} input is used to control the switch state. (See V_{CTRL} Logic Table below). The internal switching logic of the MSW2-1001ELGA is triggered by an edge on the V_{CTRL} line. For this reason, at device startup, at least one V_{CTRL} edge is required to synchronize the switch state with the V_{CTRL} input condition. (See Section 3.4 Startup Sequence) A pull-down resistor is recommended on the V_{CTRL} line to prevent floating control voltages from changing the switch state.

V_{CTRL} Logic	Active Switch Path
0	RFC to RF2
1	RFC to RF1

V_{CTRL} Logic Table

Application Circuit Description



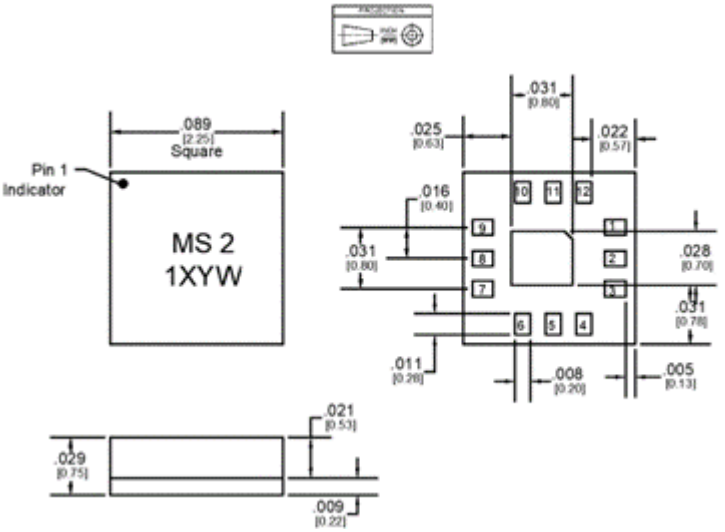
Supply bypass capacitors are placed on V_{DD} and V_{SS} supply lines to minimize supply noise and RF coupling into the switch supply circuitry. Capacitor location, value and case sizes are chosen to maximize bypassing bandwidth. The 0201 100pF capacitors should be located as close as possible to the switch to maximize high frequency bypassing. Placing the capacitors close to the switch minimizes parasitic pcb trace inductance present between the capacitor and the switch which can reduce bypassing frequency. The larger 0402 10uF capacitors are used for low frequency RF / supply-noise bypassing and can be safely placed further away and/or shared between devices.

A pull-down resistor is recommended on the V_{CTRL} line to provide a well-defined control input and minimize the chances of a voltage transient causing unexpected behavior. It is also recommended to place a high frequency bypass capacitor on the V_{CTRL} line. Similar to those on the supply lines, an 0201 100pF capacitor placed as close to the part as possible will provide the highest frequency bypassing.

Mechanical Data

Outline Drawing

Download : Outline 2D Drawing

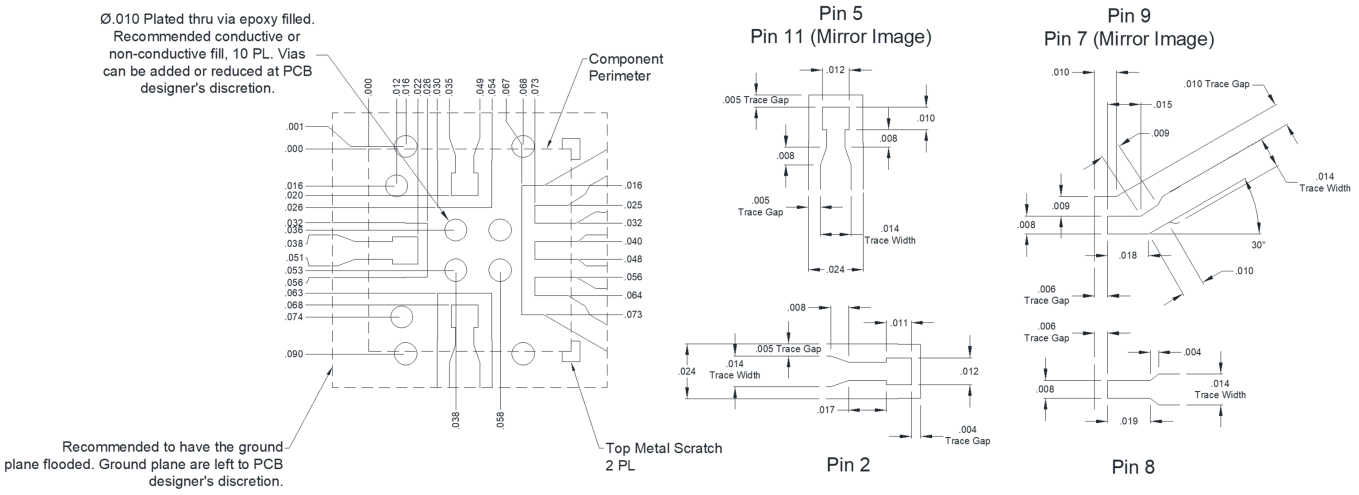


Pad #	Function
1	GND
2	RF C
3	GND
4	GND
5	RF 1
6	GND
7	VDD
8	VCTRL
9	VSS
10	GND
11	RF 2
12	GND

1. Dimensions are shown in both inches and [mm]
2. Ground paddle chamfer indicates pin 1 location
3. Plastic over-molded laminate
4. I/O Leads and ground paddle are 0.03 microns AU over 5-10 microns Ni

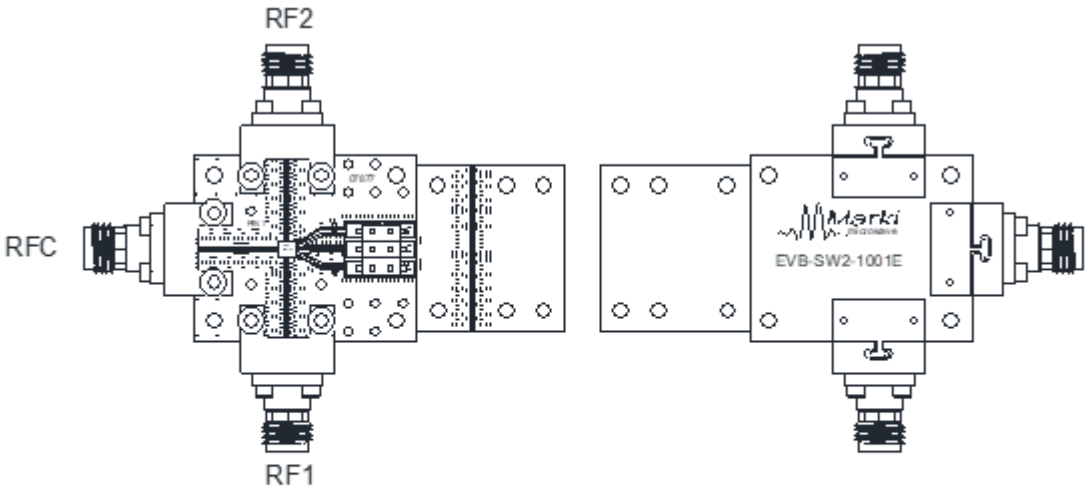
Footprint Image

Download : Footprint Drawing



The landing patterns are to be used on Rogers 4003, 0.008" thick, $\frac{1}{2}$ Oz Cu.

Evaluation Board - Outline Drawing



Port	Connector Type
RF1	2.4 mm Female
RF2	2.4 mm Female
RFC	2.4 mm Female

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